

## EXPERIMENTAL STUDY ON THE EFFECT OF MAGNETIC FIELD ON CURRENT-VOLTAGE CHARACTERISTICS OF *n*-CHANNEL ENHANCEMENT-TYPE MOSFET

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Received 20/02/2012, online 01-03-2012

**Abstract:** An experimental study is carried out to investigate the effect of magnetic field on the static current-voltage characteristics of *n*-channel enhancement-type MOSFET. It is observed that, sufficient change in drain current in the linear region of  $I_D$  versus  $V_{DS}$  curves of the device can be achieved by changing the conductivity of the channel due to Hall-field developed by the application of constant magnetic field along the perpendicular direction to the direction of drain current flow. Experimental results show that, in average 7.03 % of change in drain current can be obtained in *BS170* *n*-channel enhancement-type MOSFET due to application of  $1400 \times 10^{-4}$  Tesla constant magnetic field along the proper direction. Results are very encouraging to implement a novel sensor which can be used for current testing in deep-submicron circuits with ultra low-voltage supply (below 2 V).

**Keywords:** Hall-Effect, Magnetic Field Sensor, MOSFET, Deep-Submicron Circuits.

### I. INTRODUCTION

The Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) is core of the integrated circuit design at present time. MOSFET is also synonymous with Insulated-Gate Field Effect Transistor (IGFET) and Metal-Insulator-Semiconductor Field Effect Transistor (MISFET). This device is extensively used in low noise amplifiers and high-speed switching circuits [1-4]; it is also an important power device [5]. The basic principle of MOSFET was first patented by J. E. Lilienfeld in 1925. M. M. Atalla and D. Kahng first successfully fabricated the MOSFET in 1959 at Bell Laboratories [6-7]. After their pioneering work, enormous developments have been achieved in field of MOS devices in terms of device size and performance in last five decades. Several researchers have been devoted themselves in theoretical and experimental studies on MOS devices with the aim of improving the device performance [8-16].

In the present paper, the authors have proposed a probable magnetic field sensor based on Hall-effect which can be used for current testing in sub-micron circuits with ultra low-voltage supply, i.e. below 2 V. The effect of Hall-field developed due to application of constant magnetic field along the perpendicular direction to the direction of drain current flow in *n*-channel enhancement-type MOSFET is experimentally studied. The basic theory of the present study is presented in the next section. Experimental procedure and results are discussed in section III and section IV respectively. Finally the paper is concluded in section V.

### II. BASIC THEORY

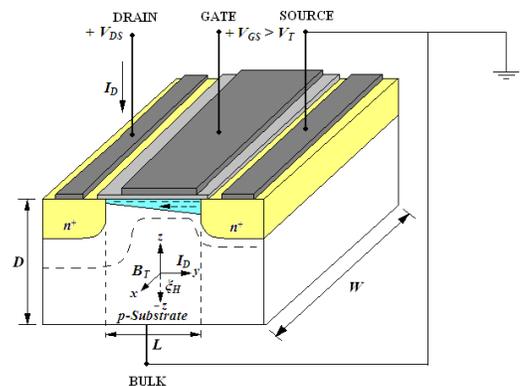
The Hall-effect is a consequence of the forces that are exerted on moving charges by electric and magnetic fields, which was discovered by Edwin Hall in 1879 [17]. If a constant magnetic

field,  $B_T$  (positive *x*-direction) is applied along perpendicular to the direction of drain current,  $I_D$  (positive *y*-direction) as shown in Figure 1, then the Hall-field,  $\zeta_H$  produced by the Hall-effect is given by [18],

$$\zeta_H = \left( \frac{p\mu_p^2 - n\mu_n^2}{e(p\mu_p + n\mu_n)^2} \right) \left( \frac{I_D}{W.T} \right) B_T \quad (1)$$

In case of *n*-channel enhancement-type MOSFET,  $I_D$  is entirely carried by majority carriers, i.e. electrons. Consequently,  $n\mu_n \gg p\mu_p$ ; thus equation (1) can be written as,

$$\zeta_H = \left( \frac{-1}{en} \right) \left( \frac{I_D}{W.T} \right) B_T \quad (2)$$



**Figure 1:** *n*-Channel Enhancement Mode MOSFET structure showing the direction of applied Magnetic Field, Drain Current and developed Hall-Field.

The Hall-field is developed along the negative *z*-direction due to accumulation of electrons at the surface of the device from the channel region as a consequent of Hall-effect. For small  $V_{DS}$  values, the channel region has the characteristics of a resistor, so the  $I_D$  can be written as [19],

$$I_D = g_d V_{DS} \quad (3)$$

where  $g_d$  is the channel conductance for  $V_{DS} \rightarrow 0$ . The channel conductance is given by,

$$g_d = \left(\frac{W}{L}\right) \mu_n |Q_n'| \quad (4)$$

Where,  $|Q_n'|$  is the magnitude of the inversion layer charge per unit area. As a result of Hall-effect, since the electrons are accumulated at the bottom surface of the device, the value of  $|Q_n'|$  is effectively reduced, which intern reduces the channel conductance and thus drain current,  $I_D$  is reduced.

If the constant magnetic field,  $B_T$  is applied along reversed direction, i.e. along negative  $x$ -direction, then the effect will be totally opposite. In that case  $g_d$  will be increased, thereby increasing  $I_D$ . But this change in magnitude of  $I_D$  due to Hall-effect is only limited to small  $V_{DS}$  values, i.e. within the linear region, where the expression of drain current is,

$$I_D = \frac{\mu_n C_{ox} W}{L} \left[ (V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \quad \text{for } 0 < V_{DS} \leq (V_{GS} - V_T) \quad (5)$$

In saturation region, the expression of drain current is,

$$I_D = \frac{\mu_n C_{ox} W}{2L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \quad \text{for } 0 < (V_{GS} - V_T) \leq V_{DS} \quad (6)$$

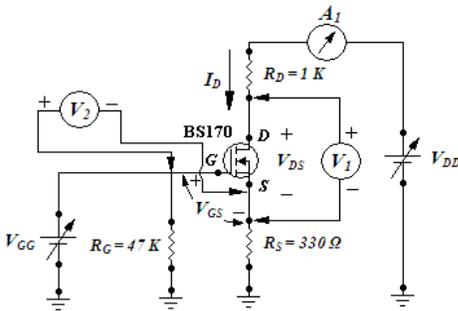
Channel conductance in saturation region is given by [20],

$$g_d = \frac{I_D \lambda}{1 + \lambda V_{DS}} \cong I_D \lambda \quad (7)$$

In long channel MOSFETs  $\lambda \approx 0$ ; therefore  $g_{ds} = 0$ . That is why in long channel MOSFETs channel conductance is independent of inversion layer charge per unit area,  $|Q_n'|$ . So, effect of magnetic field on the short-channel MOSFETs,  $\lambda \neq 0$ ; thus very minor effect may be observed in short-channel MOSFETs.

### III. EXPERIMENTAL PROCEDURE

Experiment is carried out to study the effect of magnetic field on drain current-voltage characteristics of BS170, 60V  $n$ -channel enhancement type MOSFET. Figure 2 shows the circuit diagram to plot the  $I_D$  versus  $V_{DS}$  curves for different values of  $V_{GS}$ . The variable voltage source  $V_{DD}$  is varied from zero to higher values, keeping  $V_{GG}$  at a fixed value (such that  $V_{GS} > V_{TO} = 2.1V$  for BS170). Readings of  $V_{DS}$  and corresponding drain current,  $I_D$  are taken from voltmeter  $V_1$  and milli-ammeter  $A_1$  respectively. Family of  $I_D$  vs  $V_{DS}$  curves can be plotted for different applied  $V_{GS}$  values (different values of  $V_{GS}$  can be set by varying  $V_{GG}$ ) by repeating the same above mentioned procedure.



**Figure 2:** Circuit to study the Drain Current-Voltage Characteristics of  $n$ -Channel Enhancement Mode MOSFET (BS170).

Experimental setup is shown in Figure 3 to investigate the magnetic field effect on  $I_D$  vs  $V_{DS}$  curves. Constant magnetic field is applied along positive  $x$ -direction (shown in Figure 3) by using electromagnet keeping north-pole at the back-side and south-pole at the front-side. The direction of the magnetic field can be reversed (i.e. along the negative  $x$ -direction) by just placing south-pole in place of north-pole and vice-versa. Now the  $I_D$  vs  $V_{DS}$  family of curves can be plotted following the same procedure as discussed earlier in the presence of constant magnetic field along the positive  $x$ -direction as well as the negative  $x$ -direction. Magnetic flux density,  $B_T$  can be varied by varying the constant current through the electromagnet.

### IV. EXPERIMENTAL RESULTS

The SPICE simulated and experimentally obtained  $I_D$  vs  $V_{DS}$  curves for different  $V_{GS}$  values ( $V_{GS} = 3V, 4V, 5V, 6V, 7V$ ) are shown in Figure 4. Slight disagreement between SPICE simulation and experimental results are due to the inaccuracy in the available SPICE modeling of BS170  $n$ -channel enhancement type MOSFET (DUT).

$I_D$  vs  $V_{DS}$  curves for  $V_{GS} = 4V, 5V$  and  $6V$  under constant magnetic flux density,  $B_T = 0$  Tesla,  $700 \times 10^{-4}$  Tesla and  $1400 \times 10^{-4}$  Tesla along the positive  $x$ -direction are shown in Figure 5. It can be observed that, within the linear region of  $I_D$  vs  $V_{DS}$  curves, the drain current  $I_D$  decreases as the  $B_T$  increases, but in the saturation region,  $I_D$  remains same with the increment of  $B_T$ . The behavior is in agreement with the theoretical model as discussed in section II. Due to the increment of  $B_T$  along the negative  $x$ -direction, larger Hall field,  $\zeta_H$  is developed along the negative  $z$ -axis, which in turn causes decrement in negative inversion layer charge, thereby decreasing the effective channel conductance. Consequently,  $I_D$  decreases for small values of  $V_{DS}$  (i.e. in the linear region). But in the saturation region, channel conductance is already zero for long-channel MOSFETs (BS170). That is why  $I_D$  remains unchanged in saturation region. Figure 6 shows the family of  $I_D$  vs  $V_{DS}$  curves under  $B_T = 0$  Tesla,  $700 \times 10^{-4}$  Tesla and  $1400 \times 10^{-4}$  Tesla along the negative  $x$ -direction. Due to application of constant magnetic field along negative  $x$ -direction, the Hall-field is developed along the positive  $z$ -axis. This causes larger accumulation of negative charges in the inversion layer, causing increment in channel conductance for small  $V_{DS}$  (linear region). As a result,  $I_D$  increases. But again in the saturation region, since after pinch-off the channel is constricted, so channel conductance is zero. Consequently, no change in  $I_D$  is observed in the saturation region due to application of  $B_T$  along the negative  $x$ -direction.

It is clear that, application of constant magnetic field perpendicular to the drain current direction causes change in the drain current in the linear region of MOSFET I-V characteristics. So this arrangement is well suited for designing Magnetic Field Sensor, whose sensitivity is given by,

$$S = \frac{\delta I_D}{I_D} \quad (8)$$

Where  $\delta I_D$  is the current difference between the  $I_D$  due to application of  $B_T$  and  $I_D$  due to  $B_T = 0$ , (i.e.  $\delta I_D = I_D|_{B_T} - I_D|_0$ ).

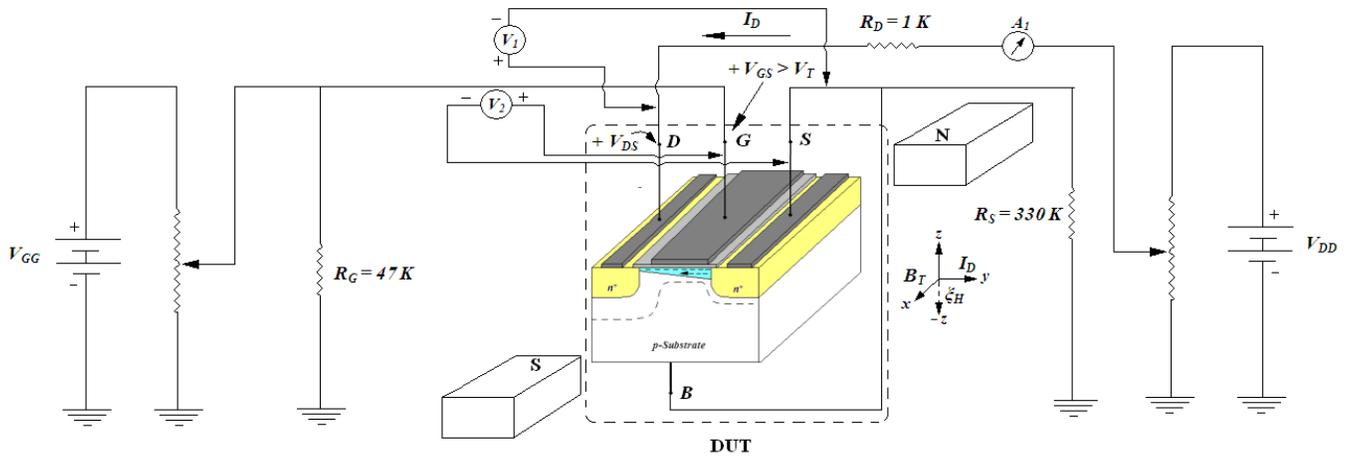


Figure 3: Experimental setup (Device Under Test [DUT] : BS170).

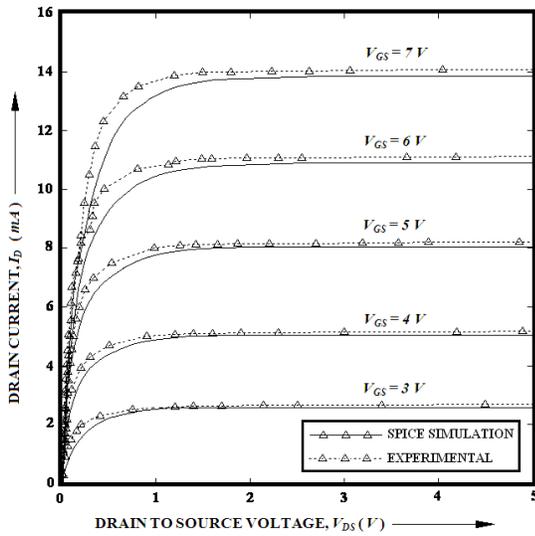


Figure 4: Experimental and SPICE Simulated Drain Current-Voltage Characteristics of *n*-Channel Enhancement-type MOSFET (BS170).

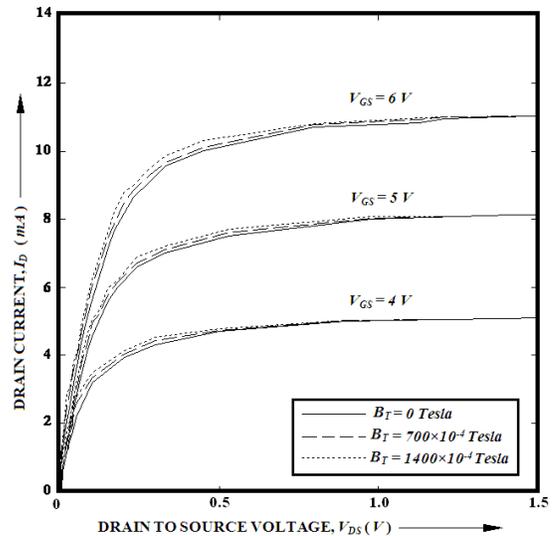


Figure 6: Variation of Drain Current-Voltage Characteristics of *n*-Channel Enhancement-type MOSFET (BS170) due to applied Magnetic Flux Density (Negative *x*-direction).

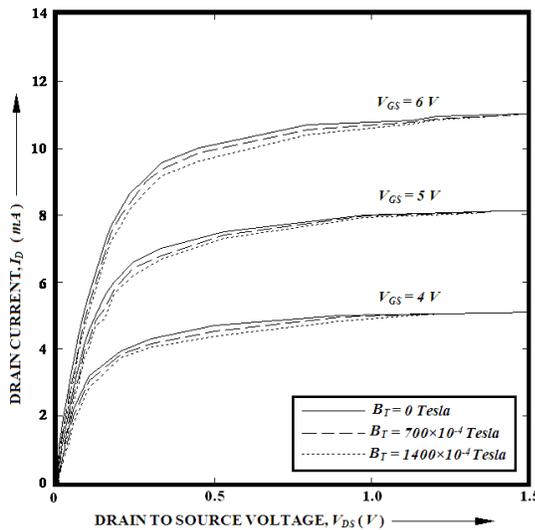


Figure 5: Variation of Drain Current-Voltage Characteristics of *n*-Channel Enhancement-type MOSFET (BS170) due to applied Magnetic Flux Density (Positive *x*-direction).

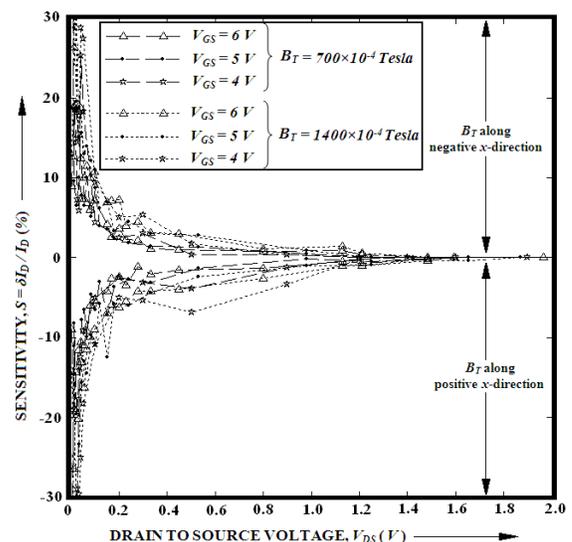


Figure 7: Variation of Sensitivity with Drain to Source Voltage at different Magnetic Flux Densities.

Sensitivity (%) of the device is plotted against drain to source voltage for different values of  $B_T$  (along positive & negative  $x$ -axis) in Figure 7. It is interesting to observe that the sensitivity of the device is very high for smaller values of  $V_{DS}$  ( $V_{DS} \rightarrow 0$ : linear region); but it gradually decays to zero when the device enters the saturation region. Experimental results show that in average 4.42% and 7.03% of the sensitivity ( $S$ ) may be achieved due to the application of  $700 \times 10^{-4}$  Tesla and  $1400 \times 10^{-4}$  Tesla of constant magnetic flux density perpendicular to the direction of drain current flow in BS170  $n$ -channel enhancement type MOSFET.

## V. CONCLUSIONS

The effect of magnetic field induced Hall-field on the drain current-voltage characteristics of  $n$ -channel enhancement type MOSFET is studied in this paper. It is noted that the drain current of the device within the linear region of its current-voltage characteristics changes due to application of magnetic field along the direction perpendicular to the direction of flow of drain current. Clearly this arrangement is very much suitable for implementation of Magnetic Field Sensors. Results are extensively encouraging to design a novel sensor which can be used for current testing in deep-submicron circuits with ultra low-voltage supply (below 2 V).

## Acknowledgement

The authors would like to thank Supreme Knowledge Foundation Group of Institutions, Sir J. C. Bose School of Engineering, Mankundu, Hooghly, W. B., India for providing excellent laboratory facilities and necessary instruments to carry out the entire experimental work.

## References

- [1] S. Ickhyun, J. Jongwook, J. H. Sauk, K. Junsoo, P. B. Gook, L. J. Duk and S. Hyungcheol, "A simple figure of merit of RF MOSFET for low noise amplifier Design", IEEE Electron Device Letters, **29**, 1380 (2009).
- [2] I. Bastos, L. B. Oliveira, J. Goes and M. Silva, "MOSFET only wideband LNA with noise cancelling and gain optimization", in proceedings of 17<sup>th</sup> International Conference on Mixed Design of Integrated Circuits and systems (MIXDES), 306 (2010).
- [3] J. Brown, "Modeling the switching performance of a MOSFET in the high side of a non-isolated buck convertor", IEEE Transaction on Power Electronics, **21**, 3 (2006).
- [4] C. Zheng, D. Boroyevich and R. Burgos, "Experimental parametric study of the parasitic inductance influence on MOSFET switching characteristics", International Power Electronics Conference, 164 (2010).
- [5] X. Yali, S. Shan, P. Shea and Z. J. Shen, "New Physical Insights on Power MOSFET Switching losses", IEEE Transaction on Power electronics, **24**, 525 (2009).
- [6] Kahng and Dawon, "Silicon-silicon dioxide field induced surface devices", Technical memorandum issued by Bell Labs, 1961.
- [7] Kahng and Dawon, "Electric Field controlled Semiconductor device", U.S. Patent no.3, 102, 230 (filed: 31 May, 1960; issued: August 27, 1963).
- [8] H. Okada, Y. Uchida, K. Arai, S. Oda and S. Matsumura, "Vertical-type amorphous-Silicon MOSFET ICs", IEEE Transaction on Electron Devices, **35**, 912 (2009).
- [9] R. H. Crawford, "Capacitive feed through calculation in MOSFET ICs" Proceeding of IEEE, **55**, 1221 (1967).
- [10] C. Yuhua, M. J. Deen and C. C. Hung, "MOSFET modeling for RF IC design", IEEE Transaction on Electron Devices, **52**, 1296 (2005).
- [11] A. Victor, T. J. Walls and K. K. Likharev, "Nanoscale Silicon MOSFETs: A Theoretical Study", IEEE Transaction on Electron Devices, **50**, 1926 (2003).
- [12] J. Appenzeller et al., "Scheme for the fabrication of ultra short channel MOSFETs", Appl Phys. Lett., **76**, 298 (2000).
- [13] B. Doris et al., "Extreme scaling with ultra thin Si channel MOSFETs", IEDM Tech. Dig., 267 (2002).
- [14] J. A. Lopez-Villanueva, P. C. Cassinello, F. Gamiz, J. Banqueri and A. J. Palma, "Effects of the inversion-layer centroid on the performance of double-gate MOSFETs", IEEE Transaction on Electronic Devices, **47**, 141 (2000).
- [15] K. Uchida, H. Watanabe, A. Kinoshita, J. Koga, T. Numata and S. Takagi, "Experimental study on carrier transport mechanism in ultra thin-body SOI  $n$ - and  $p$ -MOSFETs with SOI thickness less than 5 nm", IEDM Tech. Dig., 47 (2002).
- [16] P. Mandal and V. Viswanathan, "CMOS, OP-AMP sizing using a Geometric Programming Formulation", IEEE Transaction on Computer Aided Design of Integrated Circuits and Systems", **20**, 22 (2001).
- [17] Edwin Hall, "On a New Action of Magnet on Electric Currents", American Journal of Mathematics, **2**, 287 (1879).
- [18] D. Chattopadhyay and P. C. Rakshit, "Electronics Fundamentals and Applications", 10<sup>th</sup> edition, New Age International Limited, 33 (2010).
- [19] D. A. Neamen, "Semiconductor Physics and Devices", 3<sup>rd</sup> Edition, Tata McGraw hill Companies, 2010, p 464.
- [20] P. E. Allen and D. R. Holberg, "CMOS Analog Circuit Design", 2<sup>nd</sup> Edition Oxford University Press, New York, 89 (2004).