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THRESHOLD VOLTAGE AND DRIFT-DIFFUSION THEORY BASED DRAIN CURRENT MODEL FOR POCKET-DMG n-MOSFETS WITH INNER FRINGING FIELD

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Abstract

This paper presents an analytical threshold voltage and drain current model for pocket implanted DMG n-MOSFET. The model is derived by applying Gauss's law to a rectangular box. The model takes into account the inner fringing capacitance at both the source and the drain ends and the sub threshold drain and the substrate bias effect. Using the surface potential model the threshold voltage is estimated. The drift-diffusion theory is used for finding the sub threshold drain current and transconductance. The adequacy of the model is verified by comparing with 2D device simulator DESSIS. A very good agreement of our model with DESSIS is obtained proving the validity of our model in suppressing the short channel effects.

Keywords: Sub threshold drain current; threshold voltage; Pseudo 2-D analysis; halo doping; halo DMG MOSFET.

I. INTRODUCTION

The channel engineering techniques minimize the hot electron injection in short channel MOSFET .A dual-material gate MOSFET can supress short channel effect effectively. In the DMG MOSFET, the work function of the metal corresponding to gate1(M_1) is greater than that for gate2(M_2) and hence the threshold voltage corresponding to M_1(V_{t1}) is greater than that corresponding to M_2(V_{t2}). Due to different work functions of two gates the surface potential profile is a step function ,which ensures a reduction in the short chanel effects. The channel engineering and the gate engineering techniques are combined to form novel device structure like the Double-Halo Dual Material gate MOSFETs. An analytical expression of the threshold voltage and the sub threshold drain current of the device is also developed.

II. MODEL DESCRIPTION

The pocket implanted DMG n-MOSFET structure shown in Fig. 1 is used to develop and implement the model as in [1].

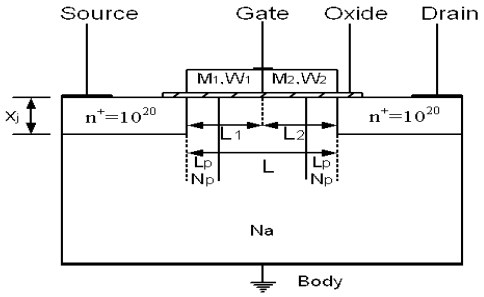

Figure (1): n-MOSFET pocket implanted DMG structure.

By applying Gauss's law to a rectangular box in the channel depletion region we get the following equation which can be analyzed analytically:

$$\varepsilon_{si}\frac{d^2\psi_s}{dx^2}-\frac{C_{ox}}{Y_d}\psi_s=qN_a-\frac{C_{ox}}{Y_d}V'_{GS} \qquad (1)$$

where $V'_{GS}=V_{GS}+V_{SB}-V'_{SB},\psi_s(x)$ is the surface potential with respect to interior of the substrate bulk, V_{SB} is the source-to-body voltage, V_{GS} is the gate-to-source voltage, t_{ox} is the gate oxide thickness, $C_{ox}=\varepsilon_{ox}/t_{ox}$ is the oxide capacitance per unit area, V_{FB} is the flat-band voltage, Y_d is the depletion layer depth and ε_{si} and ε_{ox} are the dielectric permitivities of Si and SiO_2 respectively.

The above equation can be solved as in [1] by dividing the total depletion region into different parts to get an expression of the sub threshold surface potential. The potential due to inner fringing fields are considered as in [1],[2] and [3] for finding the potentials at the source and the drain ends.

II.1 Model of threshold voltage

Using the above surface potential model,the threshold voltage V_T which is the gate voltage V_{GS} at which the minimum value of the subthreshold surface potential $\psi_{S,\min}=2*\phi_F+V_{SB}$ is found out.But $\psi_{S,\min}$ occurs at a particular value of x defined as x_{min}. For our purpose the value of V_{GS} for which the minimum value of surface potential is equal to $2*\phi_F+V_{SB}$ is found out for different channel length,substrate doping,etc.Now x_{min} corresponding to $\psi_{S,\min}$ is approximated at the junction of regions 2 and 3 or regions 3 and 4 as in [1]. Hence, an iterative numerical method is applied to find the value of threshold voltage.

II.1 Model of drain current

It is seen that the drain current I_D depends on the drain-to-source voltage V_{DS} strongly for the short channel devices.Also the conduction layer depth of the channel depends on the threshold voltage.Taking the positive direction of x as reference as in Fig-1,the drain current density is given by

$$J_n=-q*\mu_n*\phi_t\{(-n/\phi_t)*(d\psi_S/dx)+(dn/dx)\} \qquad (2)$$

Here n=inversion layer electron density,μ_n=electron mobility in inversion layer. The drift-diffusion model gives drain current density for halo-DMG n Mosfets.

$$J_n=-q*\mu_n*\phi_t*N_a*[\exp\{-\psi_S(L)/\phi_t\}-\exp\{-\psi_S(0)/\phi_t\}]/[\int_0^L\exp\{-\psi_S(x)/\phi_t\}dx] \qquad (3)$$

The effective conduction layer depth in depletion or weak inversion is given by

$$\delta=\phi_t*sqrt[\in_{Si}/\{2*q*N_a(2*\phi_{F,av}+V_{GT}/f)\}] \qquad (4)$$

where $V_{GT}=V_{GS}-V_T$. A fitting parameter f =1.25 is taken for tallying with DESSIS results[5].

Also a correction factor is required for finding the drain current given as follows.

$$\alpha=\exp[0.2*\{\{\{E_g/(2*q)\}-\phi_{F,av}\}\}/\phi_t\}^2-\{(2*(V_{GS}+V_{SB}))/(\phi_{F,av}+V_T)\}] \qquad (5)$$

The corrected drain current is obtained by integrating the current density over the cross section of the conducting channel, given as $I_{DS}=J_n*W*\delta*\alpha$ where W is the device channel width.

The transconductance g_m and I_{DS} are related by

$$\frac{g_m}{I_{DS}} = \frac{\Phi_t}{m} \qquad (6)$$

where m>1 as in [4].

Since I_{DS} is more for DHDMG and SHDMG compared to DMG,so the value of g_m is more in DHDMG than DMG.

III. RESULTS

The polysilicon gate MOSFET structure shown in Fig.1 is used to verify the surface potential model against the 2-D numerical device simulator DESSIS of ISE TCAD. The gate, source, and drain contacts of the MOSFET are made of n-type polysilicon and the body contact is made of p-type polysilicon.

Fig. 2 shows the surface potential profiles between the source and drain of a DHDMG MOSFET for L=100nm.

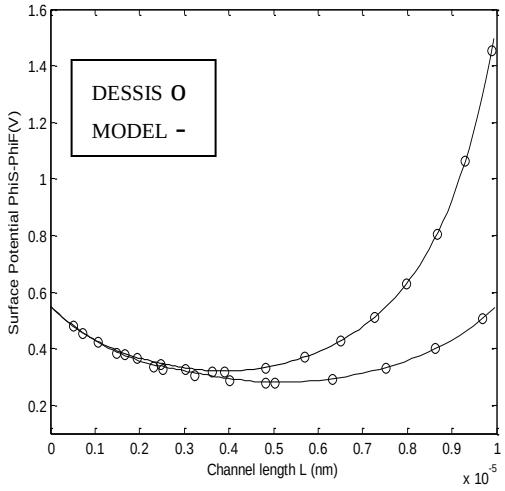

Figure (2): Surface potential profile for 100nm technology Double halo DMG MOSFET. The substrate doping concentration is $N_a = 6 \times 10^{17}$ cm^{-3} and bias voltages $V_{SB} = V_{GS} = 0$ V with two drain voltages $V_{DS} = 0$and 1 V are used. Effective channel length L=100nm

As evident from Fig. 2 a very good agreement of the proposed model (solid curve) with the DESSIS (circular symbols) is observed.

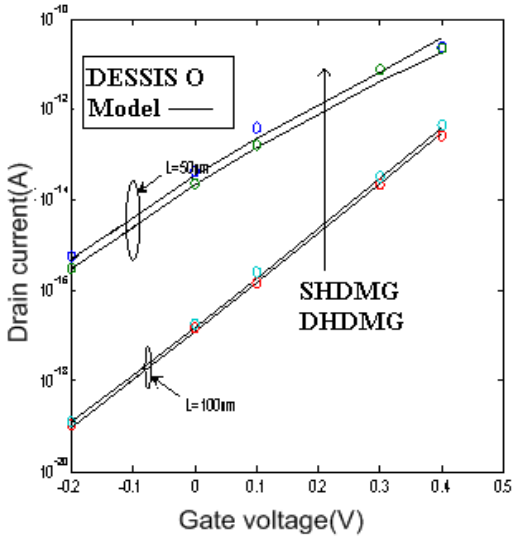

Figure (3): Comparison of subthreshold drain current versus gate bias of SHDMG and DHDMG MOSFETs for L = 50nm and 100nm with V_{DS}=1V and fixed doping of $N_a=4\times10^{17}$ and $N_p=1.2\times10^{18}$ cm^{-3} against the applied voltages V_{GS}=0 V= V_{GB} =V_{SB} .

Fig. 3 illustrates the increase in subthreshold drain current with increment in Halo implant doping.

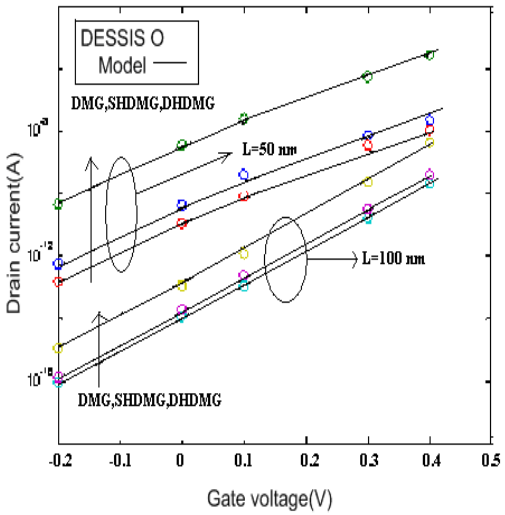

Figure (4): Comparison of subthreshold drain current versus gate bias for DMG,SHDMG and DHDMG MOSFETs for L = 50nm and 100nm with V_{DS}=0.5V and fixed doping of $N_a=4\times10^{17}$ and $N_p=1.2\times10^{18}$ cm^{-3} against the applied voltages V_{GS}=0 V= V_{GB} =V_{SB} .

It is observed from Fig. 4 that the drain current is increased in DHDMG compared to SHDMG and DMG.This is because the electron velocity increases at the source and the drain end due to the halo implants.The improvement of current in subthreshold regime makes the device suitable for low-power analog circuits.

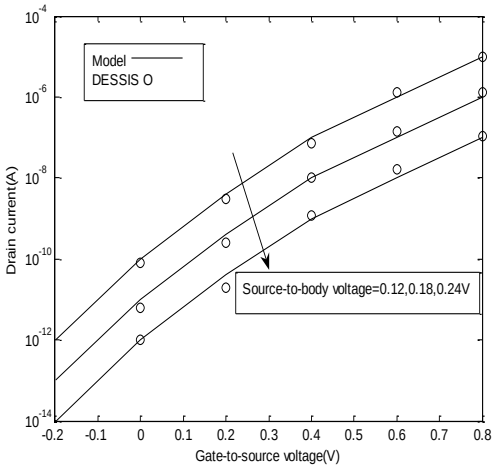

Figure (5): Drain current v/s gate voltage for L=50 nm, V_{SB}=0V,and drain voltage V_{DS} =1V with N_p =4*10^{18} cm^{-3} , N_a =1*10^{17} cm^{-3}, for three different source biases 0.12,0.18 and 0.24 V.

It is seen from Fig.5 that as the source voltage is increased the inversion layer at the channel surface is reduced, and hence for a fixed drain voltage a reduced current level is found as shown in the plots.

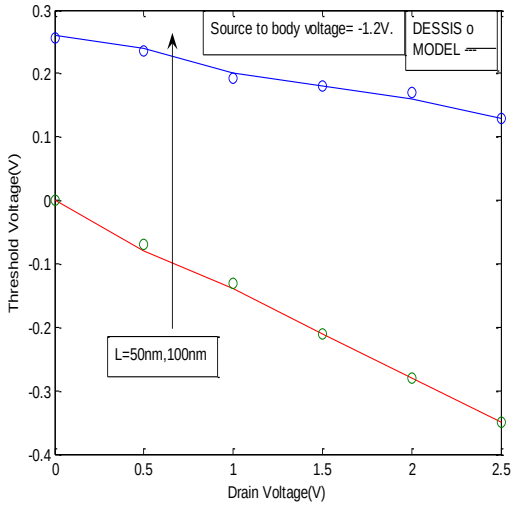

Figure (6):. Threshold voltage v/s drain voltage plots for two channel lengths L=50 nm and 100 nm for the source-to-body voltage of 0V.

The variation of the threshold voltage V_T against the drain voltage is shown in Fig. 6 for zero source-to-body voltage,with the channel length taken as 50 nm and 100 nm respectively. N_a =6*10^{17} cm^{-3} is considered under the applied bias V_{BS} =0 V and V_{DS} =0.5 V to generate these plots.

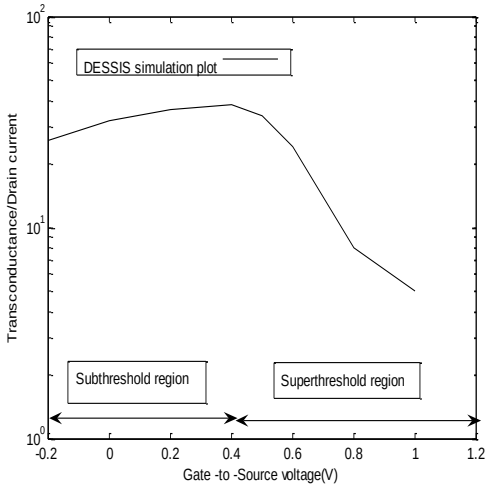

Figure (7): Plot of g_m/I_{DS} versus gate-to-source voltage for L=50 nm with V_{SB}=0V,and drain voltage V_{DS} =0.2V with N_p =1.7*10^{18} cm^{-3} , N_a =4*10^{17} cm^{-3} from DESSIS[5].

It is seen that g_m/I_{DS} is more in subthreshold regime than superthreshold as in [4]. So the gain of a circuit in the subthreshold regime is more.

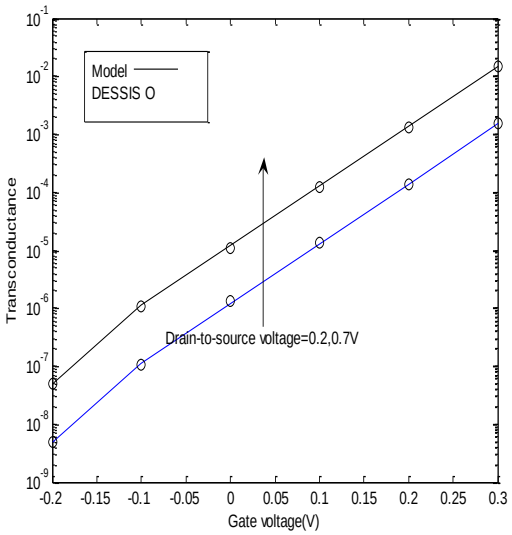

Figure (8): Plot of transconductance versus gate-to-source voltage for L=40 nm with V_{SB}=0V,and two drain voltages V_{DS} =0.2 and 0.7V with N_p =4*10^{18} cm^{-3} N_a =1.2*10^{17} cm^{-3}.

It is seen from Fig.8 that as the drain bias is increased the drain current increases. The gate control of the channel decreases and the DIBL effect is increased. Since the transconductance is proportional to the drain current so it increases.

IV. CONCLUSION

An analytical threshold voltage and drain current model for pocket implanted Dual Material Gate MOSFET is developed by solving the pseudo-2D Poisson's equation. In this model,the varying depth of channel depletion layer is accounted for along with the inner fringing potential in the source and the drain ends. The halo-DMG device shows better performance with respect to the threshold voltage and the SCE than a DMG.Based on the surface potential model the drain current and transconductance have been predicted by modifying the expression for channel conduction layer depth. Therefore this model is very useful for circuit simulation and can be applied for analyzing the MOSFET amplifiers where the device is operated in the sub threshold region.

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