Journal of Electron Devices, Vol. 12, 2012, pp. 704-712

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Journal of Electron Devices
www.jeldev.org

FRINGING CAPACITANCE BASED SURFACE POTENTIAL MODEL FOR POCKET DMG n-MOSFETs

[1] **Swapnadip De,** [2] **Angsuman Sarkar,** [3]**Chandan Kumar Sarkar, Senior Member, IEEE**
[1] ECE Dept., Meghnad Saha Institute of Technology, Nazirabad, Kolkata- 700107, India.
[2] Dept. of ECE, Kalyani Government Engineering College, Kalyani -741235, India.
[3]ETCE Dept., Jadavpur University, Kolkata-700032, India.
swapnadipde26@yahoo.co.in

Received 02/12/11, accepted 13/12/2011, online 14/12/2011

Abstract

In this paper an analytical sub threshold surface potential model of novel structures called Double pocket Dual Material Gate and Single pocket Dual Material Gate MOSFETs are presented which combines the advantages of both the channel engineering and the gate engineering techniques to effectively suppress the short channel effects. The models are derived using the pseudo 2D analysis by applying the Gauss's law to a rectangular box considering the surface potential variation with the channel depletion layer depth. The overlap and the inner fringing field capacitances at the two ends of the MOSFET are considered in our models for accurate estimation of the sub threshold surface potential. The adequacy of the model is verified by comparing with 2D device simulator DESSIS. A very good agreement of our model with DESSIS is obtained proving the validity of our model for suppressing the short channel effects.

Keywords: single pocket DMG, Surface Potential, Inner Fringing, double Pocket Doping, Gate Engineering

I. INTRODUCTION

For more than last thirty years, VLSI technology advancement has followed a path of constant shrinking of the device geometries. Over the years various methods have been proposed for reducing the MOSFET dimension keeping a constant electric field in the device. However, the voltages in the device have not shrunk as the physical dimensions which leads to the higher electric fields causing the hot electron injection into the gate.Using the channel engineering techniques ,the hot electron injection can be minimized. In order to minimize hot electron effect and to give more control of the gate over the conductance of the channel so as to increase gate transport efficiency a dual material gate structure has been proposed. The short channel efffects can primarily be attributed to the reduction of the gate control over the channel. In the DMG MOSFET, the work function of the metal corresponding to gate1(M1) is greater than that for gate2(M2) and hence the threshold voltage corresponding to M1(V_{t1}) is greater than that corresponding to M2(V_{t2}). This has the inherent advantage of improved gate transport efficiency by modifying the electric field profile along the channel. Due to different work functions of two gates the surface potentail profile is a step function ,which ensures a reduction in the short chanel effects and screening of the channel region under M1 from the drain potential variations.

To reduce the short channel effects, the channel engineering approach like single-pocket(SH) also known as lateral asymmetric channel(LAC) or double-pocket(DH) implants are used. The gate control over the channel is affected by the proximity of the source/drain due to the interaction of the depletion layers around them, particularly when the width of these depletion layers becomes comparable to the channel length. It may be noted that such sharing of gate control is the origin of the Short Channel Effects. The basic principle of the LAC or DH devices is to keep these depletion layers at minimum width by increasing the substrate doping at the source or both ends respectively.

The channel engineering and the gate engineering techniques are combined to form novel device structure like Single-pocket Dual Material Gate MOSFET and Double-pocket Dual Material gate MOSFETs has been proposed in this paper.

Surface potential can be accurately predicted by solving the Poisson's equation along the entire channel region. This requires numerical solutions which are not suitable for use in circuit analysis as the solution does not contain finite number of terms in closed form and also the computation time requirement is high. Analytical models are used as an

alternative to get solutions which are approximate but computationally efficient, so making it more convenient for understanding the device physics and handy for device design.

In a different approach called pseudo two-dimensional analysis Gauss's law is applied to a rectangular box covering the entire channel depletion region . Among the various methods of solving the Poisson's equation, this method produces a simpler manageable one-dimensional analytical expression retaining the two-dimensional accuracy to a greater extent.

As the device dimension is reduced, the various leakage capacitances and the fringing capacitances at two ends of MOSFET play an important role in the expression of sub threshold surface potential.

A simple expression for the parasitic inner fringing capacitance from the bottom edge of the gate electrode is considered and the charges induced in the source and the drain regions due to these capacitances are considered. The surface potential increases along the channel due to these charges. An accurate model of sub threshold surface potential is proposed for Double pocket Dual Material gate and Single pocket Dual Material gate MOSFETs taking into account the fringing fields at the source and drain ends and also the potential arising due to the overlap capacitances at the two ends. The models are verified with the 2D device simulator DESSIS. Very good agreements of our models with DESSIS are obtained.

II. MODEL DESCRIPTION

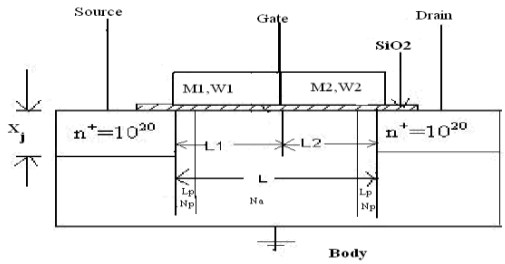


Figure 1 An n-channel Double pocket DMG-MOSFET structure.

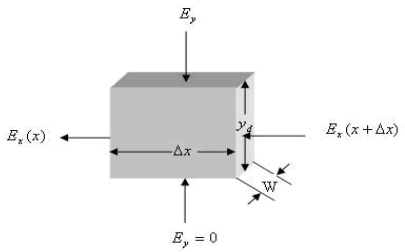


Figure 2 A rectangular Gaussian Box in the entire depletion region.

An n-channel Double-pocket DMG-MOSFET structure is shown in Fig. 1.By applying Gauss's law to the box shown in Fig.2 and neglecting the inversion layer charges in the channel depletion region, a pseudo-2D Poisson's equation can be obtained as follows:

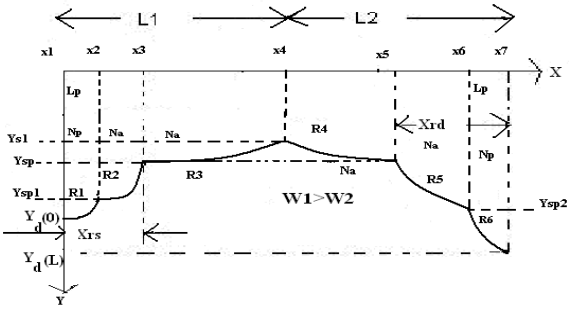
$$\varepsilon_{si}\frac{d^2\psi_s}{dx^2}-\frac{C_{ox}}{Y_d}\psi_s=qN_a-\frac{C_{ox}}{Y_d}V_{GS}' \quad \ldots \qquad (1)$$

where the symbols have their usual significances[1]. The flat-band voltages for the gate metals are given by

$V_{FB1}=(W_1 - W_{si})/q.$

$V_{FB2}=(W_2 - W_{si})/q.$

where W1 and W2 are the work functions of the gate metals and Wsi that of the silicon substrate respectively.It is considered that $W_1>W_2$.



F Figure 3 Typical variation of the depletion layer depth $Y_d(x)$.

The typical variation of depletion layer depth for the Double pocket Dual Material Gate MOSFET is shown in Fig. 3.

The fringing capacitances originate from the portion of the field lines originating from the gate electrode and terminating on the drain and source junctions. For long channel MOSFET the inner fringing capacitance effects are negligible but for short channel devices their contributions are considerable. For the subthreshold surface potential estimation the inversion layer is assumed to be negligible and as a result the horizontal field components of the electric field from the drain is assumed to be constant.The fringing capacitance in the absence of an inversion layer charge is constant and is approximately given by [9],

$$C_f=\frac{2\varepsilon_{si}W}{\pi}\ln\left[1+\frac{X_j}{t_{OX}}Sin\left(\frac{\pi}{2}\frac{\varepsilon_{ox}}{\varepsilon_{si}}\right)\right] \quad \ldots\ldots (2)$$

Where ε_{ox} and ε_{si} are the dielectric constants of oxide and silicon, respectively, W is the channel width, L is the effective channel length, t_{ox} is the oxide thickness and X_j is the depth of the source and the drain junctions. For example the contribution of the fringing capacitance C_f to the gate-to-drain capacitance C_{gd} is represented by [10],

$$C_{gdf}=C_f\left(1-\frac{2C_{gd}}{C_0}\right)\ldots\ldots (3)$$

$$C_0=WL\frac{\varepsilon_{ox}}{t_{ox}} \quad \ldots. (4)$$

Where C_0 is the total gate-to-oxide capacitance. The use of equation (3) satisfies the boundary conditions for $V_D=0$ where V_D=Drain voltage For $V_D=0$, $C_{gd}=0.5C_0$ and hence $C_{gdf}=0$

The vanishing of fringing capacitance in the linear region is the result of the high carrier concentration in the channel which isolates the drain junction from the filed lines originating from the gate electrode. The fringing and the overlap potential as a result of this capacitance at the source and the drain end are calculated using Coulomb's law.

A good model must take into account the Fringing effect also for perfect estimation of surface potential.We give a brief account of the Fringing capacitances first and then introduce theFringing potential due to inner fringing capacitance in the model .

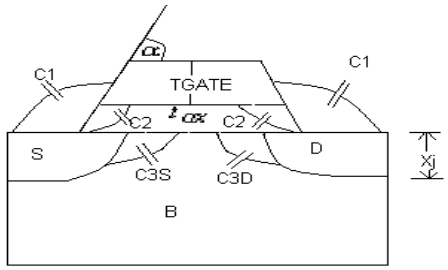


Figure 4 Fringing Capacitance Components C1, C2 and C3 are shown.

The fringing capacitance components C1, C2 and C3 are shown in Fig. 4.

C1 is the outer-fringing-field capacitance between the gate and the source or the drain electrode. C2 is the direct overlap capacitance between the gate and the source or the drain junction. C3 is the inner-fringing-field capacitance between the gate and the side wall of the source or drain junction. For C1, C2, and C3, we have the following equations:

$$C1 = W.\frac{\varepsilon_{ox}}{\alpha} - \log_e\left(1+\frac{T_{GATE}}{t_{OX}}\right) \quad ....(5)$$

$$C2 = W.\frac{\varepsilon_{ox}}{t_{OX}}\left(LD + 0.5t_{OX}\right).\left(\frac{1-\cos\alpha}{\sin\alpha} + \frac{\cos\delta}{\sin\delta}\right) \quad ..... (6)$$

Where $\delta = 0.5.\pi.\frac{\varepsilon_{ox}}{\varepsilon_{si}}$ ---------- (7)

Where α is the slanting angle of gate electrode in radians. T_{GATE} is the thickness of the gate electrode and LD is the metallurgical lateral diffusion of source, drain junction as shown in Fig.4. C_F is the maximum value of the inner-fringingcapacitancecomponentC3[11].

$$C_F = W.\frac{\varepsilon_{ox}}{\delta}.\log_e\left(1+\frac{X_j \sin\alpha}{t_{OX}}\right) \quad ...(8)$$

The capacitance component C3 is bias-dependent and it is modeled as a charge based form. Hence:

$$Q_{D.F} = -C_F.\frac{V_{DS} - VDS}{1+\exp\left(-\frac{V_{GB}-V_{FB}}{30\phi_t}\right)} = -C_F.V_{fd} \text{ --- (9)}$$

$$Q_{S.F} = -C_F.\frac{V_{GST} - V_{GS} + V_{FB} + 2\phi_F + \gamma\sqrt{2\phi_F - V_{BS}}}{1+\exp\left(-\frac{V_{GB}-V_{FB}}{30\phi_t}\right)} = -C_F.V_{fs} \quad -$$

(10)

VDS is obtained from [11].Here V_{fs} is the inner fringing potential in the source end and V_{fd} is the inner fringing potential in the drain end. It is evident that due to the inner fringing capacitances C3S and C3D an electric field is created between the source and the drain.

A model is proposed taking the varaiation of depletion layer width as $Y_d(x) = (ax+b)^2$ where the source and the drain end values are given by

$Y_d(0) = X_j + \sqrt{2\varepsilon_{si}(V_1)/(qN_P)} = X_j + X_{rs}$ and

$Y_d(L) = X_j + \sqrt{2\varepsilon_{si}(V_7)/(qN_P)} = X_j + X_{rd}$

respectivelywhere, $V_1 = V_{SB} + V_{fs} + V_{fso} + V_{bi}$, $V_7 = V_{DB} + V_{fd} + V_{fdo} + V_{bi}$, V_{bi} is the built-in potential of the substrate. V_{SB} and V_{DB} are the source and the drain bias respectively, N_a is the acceptor ion concentration, V_{fso} is the potential due to overlap capacitances at the source end and V_{fdo} is the potential due to overlap capacitances at the drain end

$X_{rs} = \sqrt{2\varepsilon_{si}(V_1)/(qN_P)}$ and

$X_{rd} = \sqrt{2\varepsilon_{si}(V_7)/(qN_P)}$

are the depth of penetrations of the depletion layers into the channel / substrate due to the built-in potential V_{bi} (between the n^+ -source/drain and the p-type channel/substrate) and the reverse bias V_{SB} and V_{DB} at the source and the drain ends . The channel is divided into six regions R_1, R_2, R_3, R_4, R_5, R_6 with the known values at the two ends as shown in Fig-3. However, near the two ends of the channel due to various fringing effects and the leakage capacitances, a large number of field lines from the source/drain are mapped on the space charge region below the source/drain outside the rectangular gauusian box .Hence a reduced value of the depletion layer depth needs to be considered near the channel. Two bias depenedent fitting parameters

$\zeta_s = 1.5V_1 / V_{bi}$ for the source end and

$\zeta_d = 1.5V_7 / V_{bi}$ for the drain end are considered for obtaining a best fit model of surface potentail profile with ISE TCAD. ζ_s and ζ_d takes into account the other fringing and the overlap capacitances at the drain and the source end. In other words, while computing a and b we use $Y_d(o) / \zeta_s$ and $Y_d(L) / \zeta_d$, instead of, $Y_d(0)$ and $Y_d(L)$ respectively.

The depth of the depletion layer(y) for the six regions are as follows:

Region-I : $x_1 = 0 < x \le x_2 = L_p$ The corresponding y values are

$y_1 = \left\{X_j + \sqrt{2\varepsilon_{si}V_1/(qN_P)}\right\}/\varsigma_s$ and

$y_2 = Y_{sp1} = \sqrt{2\varepsilon_{si}\psi_{sp1}/(qN_P)}$ with the end potentials V_1 given and V_2 to be evaluated where

$$\psi_{sp1} = \left(-\gamma_p/2 + \sqrt{\gamma_p^2/4 + V_{GB} - V_{FBP1}}\right)^2$$

$\gamma_p = \sqrt{2q\varepsilon_{si}N_p}/C_{ox}$, $V_{FBP1} = V_{FBP} - V_{FB1}$ and

$V_{FBP} = -0.56 - \varphi_t \ln(N_P/n_i)$

Region-II: $x_2 < x \le x_3 = x_{rs}$: The corresponding y values are $y_2 = Y_{sp1}$ and

$y_3 = Y_{sp} = \sqrt{2\varepsilon_{si}\psi_{sp}/(qN_P)}$

where $\psi_{sp} = \left(-\gamma_p/2 + \sqrt{\gamma_p^2/4 + V_{GB} - V_{FBP}}\right)^2$

Region-III : $x_3 < x \le x_4 = L1$: The corresponding y values are $y_3 = Y_{sp}$ and $y_4 = Y_{s1} = \sqrt{2\varepsilon_{si}\psi_1/(qN_a)}$

where $\psi_1 = \left(-\gamma/2 + \sqrt{\gamma^2/4 + V_{GB} - V_{FB1}}\right)^2$

$\gamma = \sqrt{2q\varepsilon_{si}N_a}/C_{ox}$

Region-IV : $x_4 < x \le x_5 = (L1+L2)0.65$:The corresponding y values are $y_4 = Y_{s1}$ and $y_5 = Y_{sp}$

Region-V : $x_5 < x \le x_6 = L - L_P$: The corresponding y values are $y_5 = Y_{sp}$ and $y_6 = Y_{sp2} = \sqrt{2\varepsilon_{si}\psi_{sp2}/(qN_P)}$

where $\psi_{sp2} = \left(-\gamma_p/2 + \sqrt{\gamma_p^2/4 + V_{GB} - V_{FBP2}}\right)^2$,

$V_{FBP2} = V_{FBP} - V_{FB2}$

Region-VI : $x_6 < x \le x_7 = L$: The corresponding y values are $y_6 = Y_{sp2}$ and $y_7 = \left\{X_j + \sqrt{2\varepsilon_{si}V_7/(qN_P)}\right\}/\varsigma_d$

The surface potential $\Psi_s(x)$ for all the five regions can be determined as in [1,2,3,8]. Applying the continuity of the Electric Field along the lateral direction ($d\Psi_s/dx$) at the interfaces of the various regions we get :

$a_{11}V_2 + a_{12}V_3 + a_{13}V_4 + a_{14}V_5 + a_{15}V_6 = A_1$
$a_{21}V_2 + a_{22}V_3 + a_{23}V_4 + a_{24}V_5 + a_{25}V_6 = A_2$
$a_{31}V_2 + a_{32}V_3 + a_{33}V_4 + a_{34}V_5 + a_{35}V_6 = A_3$
$a_{41}V_2 + a_{42}V_3 + a_{43}V_4 + a_{44}V_5 + a_{45}V_6 = A_4$
$a_{51}V_2 + a_{52}V_3 + a_{53}V_4 + a_{54}V_5 + a_{55}V_6 = A_5$

where the unknown voltages V_2, V_3, V_4, V_5 and V_6 are computed as in [1,2,3,8].

The same model is applied for Single-Pocket Dual Material gate MOSFET , the structure of which is shown in Fig-5. Again Gauss's law is applied to a rectangular box covering the entire depletion region and the typical variation of the depletion layer depth is shown in Fig-6.

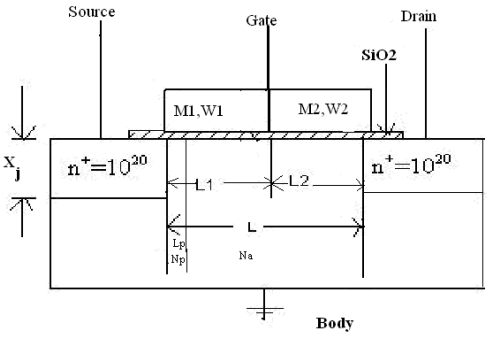


Figure 5 The structure of the n-channel single-pocket DMG-MOS transistor.

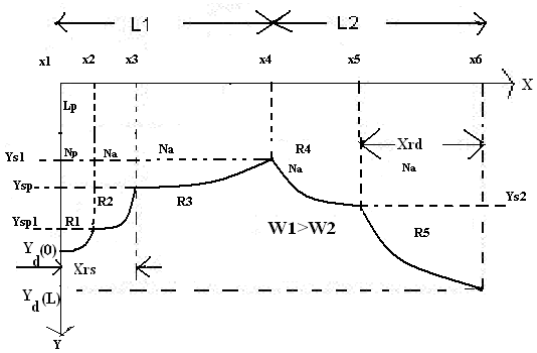


Figure 6 Typical variation of the depletion layer depth $Y_d(x)$.

The channel is divided into five regions R_1, R_2, R_3, R_4, R_5 with known values at the two ends with the source and the drain end values given by

$Y_d(0) = X_j + \sqrt{2\varepsilon_{si}(V_1)/(qN_P)} = X_j + X_{rs}$ and

$Y_d(L) = X_j + \sqrt{2\varepsilon_{si}(V_6)/(qN_a)} = X_j + X_{rd}$

respectively where, $V_1 = V_{SB} + V_{fs} + V_{fso} + V_{bi}$,

$V_6 = V_{DB} + V_{fd} + V_{fdo} + V_{bi}$.

The five regions in which the channel is divided are as follows:

Region-I : $x_1 = 0 < x \le x_2 = L_p$ The corresponding y values are $y_1 = \left\{X_j + \sqrt{2\varepsilon_{si}V_1/(qN_P)}\right\}/\varsigma_s$ and

$y_2 = Y_{sp1} = \sqrt{2\varepsilon_{si}\psi_{sp1}/(qN_P)}$ with the end potentials $V_1 = V_{bi} + V_{SB}$ and V_2 to be evaluated $\psi_{sp1} = \left(-\gamma_p/2 + \sqrt{\gamma_p^2/4 + V_{GB} - V_{FBP1}}\right)^2$,

$\gamma_p = \sqrt{2q\varepsilon_{si}N_p}/C_{ox}$, $V_{FBP1} = V_{FBP} - V_{FB1}$ and

$V_{FBP} = -0.56 - \varphi_t \ln(N_P/n_i)$

Region-II : $x_2 < x \le x_3 = x_{rs}$: The corresponding y values are $y_2 = Y_{sp1}$ and $y_3 = Y_{sp} = \sqrt{2\varepsilon_{si}\psi_{sp}/(qN_P)}$

where $\psi_{sp} = \left(-\gamma_p/2 + \sqrt{\gamma_p^2/4 + V_{GB} - V_{FBP}}\right)^2$

Region-III : $x_3 < x \leq x_4 = L1$: The corresponding y values are $y_3 = Y_{sp}$ and $y_4 = Y_{s1} = \sqrt{2\varepsilon_{si}\psi_1 / (qN_a)}$

where $\psi_1 = \left(-\gamma/2 + \sqrt{\gamma^2/4 + V_{GB} - V_{FB1}}\right)^2$

$$\gamma = \sqrt{2q\varepsilon_{si}N_a} / C_{ox}$$

Region-IV : $x_4 < x \leq x_5 = (L1+L2)0.75$: The corresponding y values are $y_4 = Y_{s1}$ and

$y_5 = Y_{s2} = \sqrt{2\varepsilon_{si}\psi_2 / (qN_a)}$

where $\psi_2 = \left(-\gamma/2 + \sqrt{\gamma^2/4 + V_{GB} - V_{FB2}}\right)^2$

Region-V : $x_5 < x \leq x_6 = L$: The corresponding y values are $y_5 = Y_{s2}$ and

$y_6 = \left\{X_j + \sqrt{2\varepsilon_{si}V_6 / (qN_a)}\right\} / \varsigma_d$

The surface potential $\Psi_s(x)$ for all the five regions can be determined as in [1,2,8]. Applying the continuity of the Electric Field along the lateral direction ($d\Psi_s/dx$) at the interfaces of the various regions we get :

$a_{11} V_2 + a_{12} V_3 + a_{13} V_4 + a_{14} V_5 = A_1$
$a_{21} V_2 + a_{22} V_3 + a_{23} V_4 + a_{24} V_5 = A_2$
$a_{31} V_2 + a_{32} V_3 + a_{33} V_4 + a_{34} V_5 = A_3$
$a_{41} V_2 + a_{42} V_3 + a_{43} V_4 + a_{44} V_5 = A_4$

The corresponding depth of depletion layers are obtained as in the case of Double-Pocket Dual Material Gate MOSFET. The surface potential $\Psi_s(x)$ for all the five regions are determined as in [1,2,8]. The fitting parameters used in this case are same as in case of Double-Pocket Dual Material gate MOSFET.

III. RESULTS

The proposed structure shown in Fig 1 is used to verify the model against the 2-D numerical device simulator DESSIS.Two different metals M_1 and M_2 are used.The typical parameters for the oxide thickness,the junction depth and the channel length are t_{ox}=3.5 nm,X_j =40 nm and L=100 nm which are representative for a typical 130-nm device,along with V_{SB}=0V are used.Similarly unless otherwise specified,equal values for L_1 and L_2 with typical work functionsW_1=4.25 eV and W_2=4.1 eV are used in this study.Solid lines are used for the model predictions,while the circular symbols are used for the corresponding predictions by DESSIS.

Fig 7, 8 and 9 shows the comparison of the subthreshold surface potential profiles generated by our model and the DESSIS,against the variation of the substrate and pocket doping.All the plots show a convincing agreement of the model with DESSIS,for a wide variation of the device length,the substrate doping and the drain voltage,in addition to nonzero voltages on the source and the gate terminals.The influence of varying the work function of the two gate materials on the potential profiles are then studied.

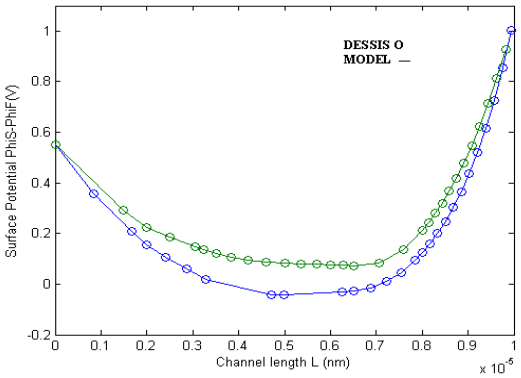


Figure7 The plots for two different values of the substrate doping N_a=4×10^{17} and 1×10^{17} cm^{-3} against the applied voltages V_{GS}=0 V= V_{GB} =V_{SB} and V_{DS}=0.5 V.

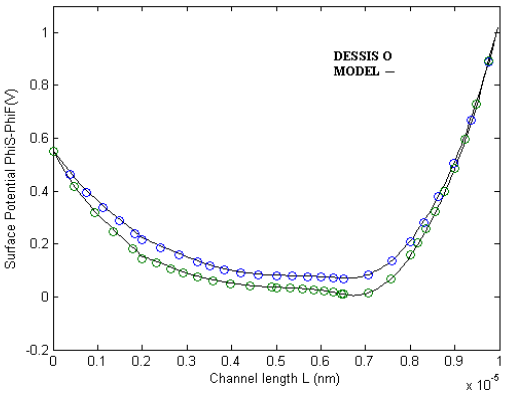


Figure 8 The plots for two different values of the pocket doping N_p=1.2×10^{18} and 1.8×10^{18} cm^{-3} against the applied voltages V_{GS}=0 V= V_{GB} =V_{SB} and V_{DS}=0.5 V, N_a=1×10^{17} cm^{-3}

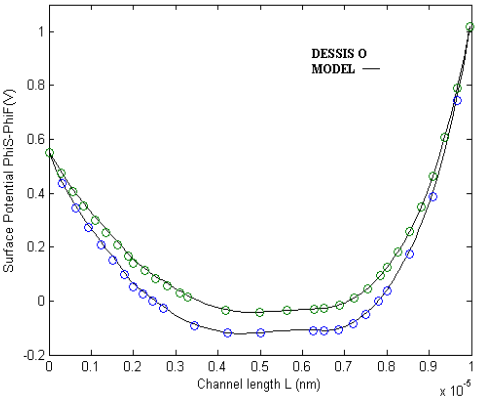


Figure 9 The plots for two different values of the substrate and pocket doping N_p=1.8×10^{18},N_a=6×10^{17}cm^{-3} andN_p=1.2×10^{18} , N_a= 4×10^{17} cm^{-3}against the applied voltages V_{GS}=0 V= V_{GB} =$V_{SB}$and V_{DS}=0.5 V.

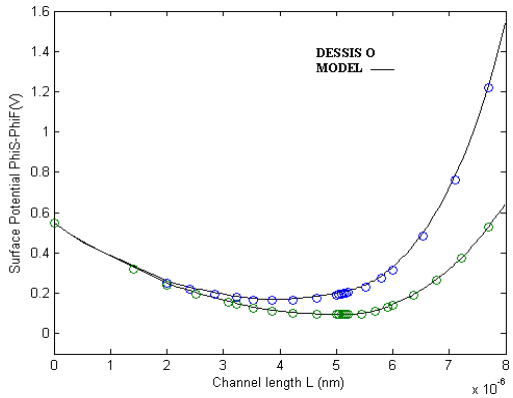


Figure 10 Plots for different values of V_{DS}=1V, 0.1Vwith $N_p=1.2\times10^{18}$,$N_a=1\times10^{17}cm^3$against the applied voltages V_{GS}=0V= V_{GB} =V_{SB} ,L=80 nm.

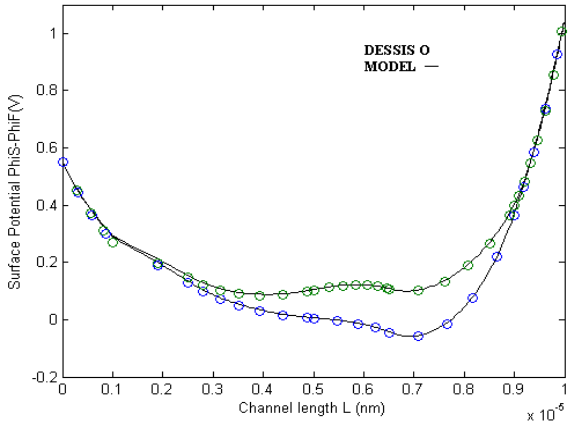


Figure11The potential profiles for two sets of gate materials W_1=4.3 and W_2=4.1 and W_1=4.2and W_2=3.9 for L=100 nm,$N_p=2\times10^{18}$,$N_a=1\times10^{17}cm^{-3}$against the applied voltages V_{GS}=0 V= V_{GB} =V_{SB}, V_{DS}=0.5V.

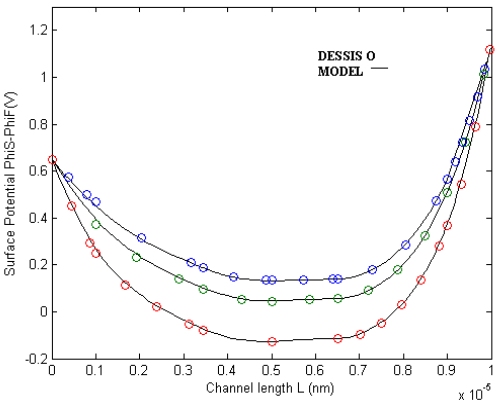


Figure12 The potential profiles for three sets of gate biasa)V_{GS}=0.1V,V_{GB}=0.2V,V_{SB}=0.1V b)V_{GS}=0V,V_{GB}=0.1V,V_{SB}=0.1Vc)V_{GS}=-0.2V, V_{GB}=-0.1V,V_{SB}=0VforL=100nm $N_p=1.2\times10^{18}$,$N_a=4\times10^{17}cm^{-3}$,$V_{DS}$=0.5V.

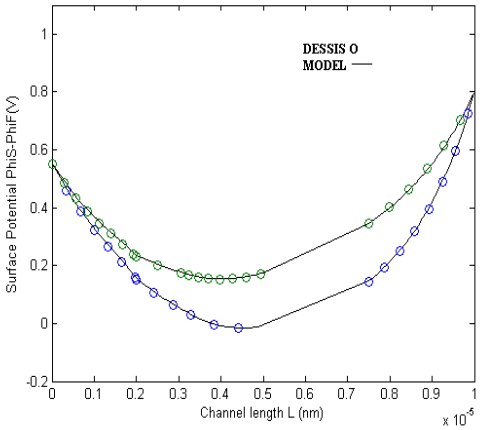


Figure 13 The plots for two different values of the substrate doping $N_a=4\times10^{17}$ and 1×10^{17} cm^{-3} against the applied voltages V_{GS}=0 V= V_{GB} =V_{SB} and V_{DS}=0.25 V.

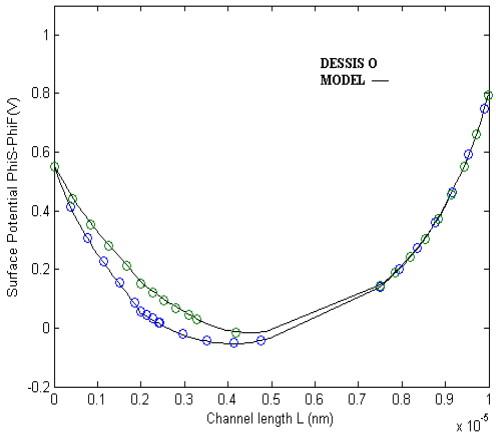
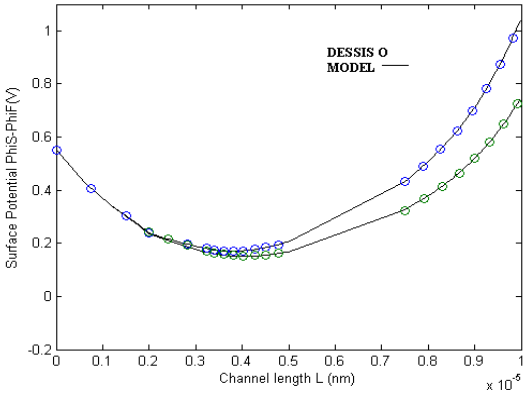


Figure 14 The plots for two different values of the pocket doping $N_p=2.2\times10^{18}$ and 1.2×10^{18} cm^{-3} against the applied voltages V_{GS}=0 V= V_{GB} =V_{SB} and V_{DS}=0.25 V, $N_a=4\times10^{17}$ cm^{-3}

Fig 10,11,12,13,14 shows the comparison of the subthreshold surface potential profiles for Double Pocket Dual material Gate MOSFET generated by our model and the DESSIS,against the variation of the drain bias, two different gate materials and gate bias, substrate doping, Pocket doping. Fig 15 and 16 shows the comparison of the subthreshold surface potential profiles for Single Pocket Dual material Gate MOSFET generated by our model and the DESSIS,against the variation of the drain bias and two different gate materials. A good agreement of the model calculation with DESSIS proves that the model can be applied for any combinations of the gate material work functions and/or lengths.



F Figure 15 The plots for two different values of V_{DS} = 0.5V and 2V, considering $N_p = 1.2\times10^{18}$, $N_a=1\times10^{17}$ cm^{-3} against the applied voltages V_{GS} = 0V = V_{GB} =V_{SB}, L=100 nm.

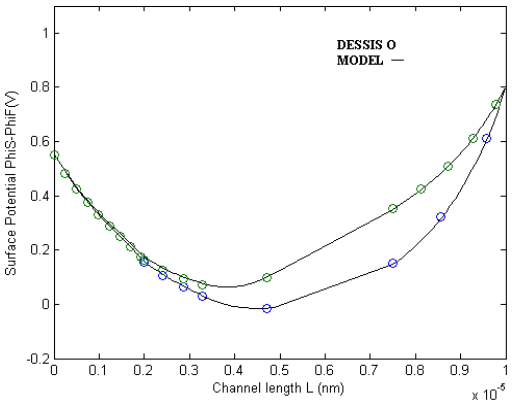


Figure 16 The potential profiles for two sets of gate materials W_1=4.25 and W_2=4.1 and W_1=4.2and W_2=3.76 for L=100 nm,$N_p=1.2\times10^{18}$,$N_a=4\times10^{17}cm^{-3}$against the applied voltages V_{GS}=0 V= V_{GB} =V_{SB}, V_{DS}=0.25V.

Again the same procedure is followed for Single Pocket Dual Material Gate MOSFET shown in Fig 5 with the substrate and pocket doping varied.Also the results obtained for two sets of gate materials are shown.The results obtained are again compared with that of the 2-D numerical device simulator DESSIS.A good agreement of the model calculations with DESSIS are obtained. Fig 17 and 18 shows the comparison of the subthreshold surface potential profiles for SHDMG and the DESSIS,against the variation of the substrate doping,the channel length and the drain voltage.

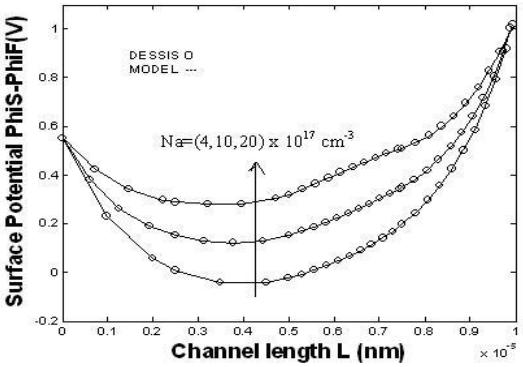


Figure 17 The plots for three different values of the substrate doping $N_a=4\times10^{17}$,10^{18} and 2×10^{18} cm^{-3} against the applied voltages V_{GS}=0 V and V_{DS}=0.5 V for SHDMG.

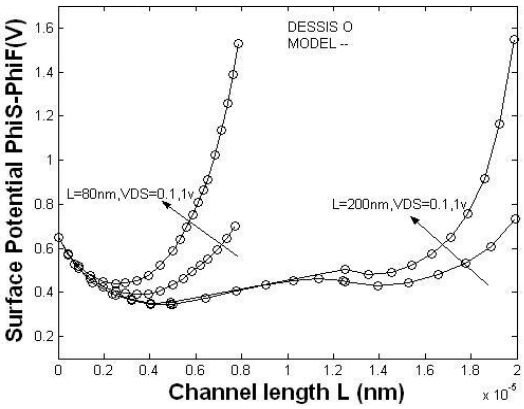


Figure. 18 The variation of the potential profiles in an SHDMG device with two different channel lengths L=80 and 200 nm for $N_a=6\times10^{17}$ cm^{-3} against two different drain voltages V_{DS}=0.1 V and 1 V along with V_{SB}=0.1 V and V_{GB}=0.2 V.

All the plots show a convincing agreement of the model with DESSIS,for a wide variation of the device length,the substrate doping and the drain voltage,in addition to nonzero voltages on the source and the gate terminals.

The influence of varying the work function and the length of the two gate materials on the potential profiles are then studied.The corresponding potential profiles in a device with $N_a=6\times10^{17}$ cm^{-3} , V_{DS}=0.5 V and the grounded gate terminal are plotted.

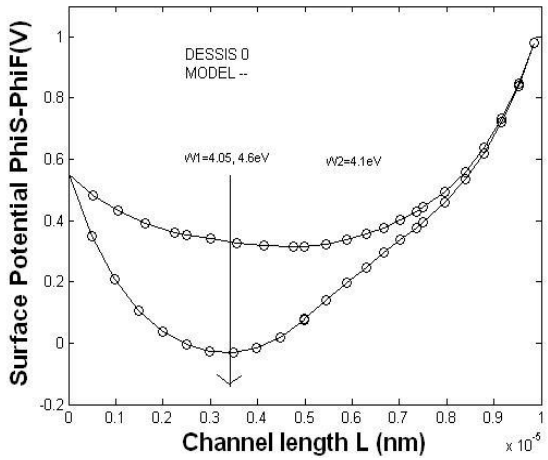


Figure 19 The SHDMG potential profiles for a fixed value of W_2=4.1 eV,with two different values of W_1=4.05 and 4.6 eV,respectively.

When the length of the gate materials are changed for fixed work function values,we get the plots shown in Fig 21 for two sets of material length.In one of them,L_1=25 nm and L_2=75 nm,while just the reverse values i.e., L_1=75 nm and L_2=25 nm are used for the other set.

A good agreement of the model calculation with DESSIS proves that the model can be applied for any combinations of the gate material work functions and/or lengths.

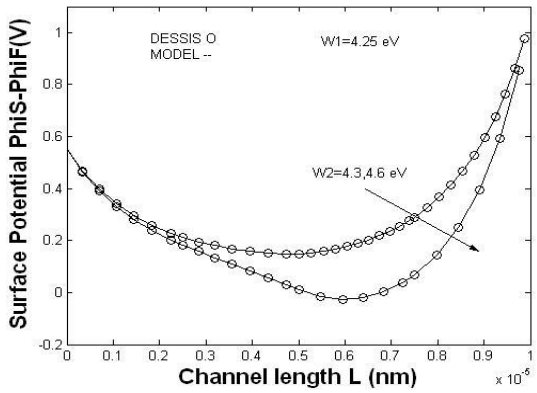


Figure. 20 The SHDMG potential profiles for a fixed value of W_1=4.25 eV with two different values of W_2=4.3 and 4.6 eV,respectively.

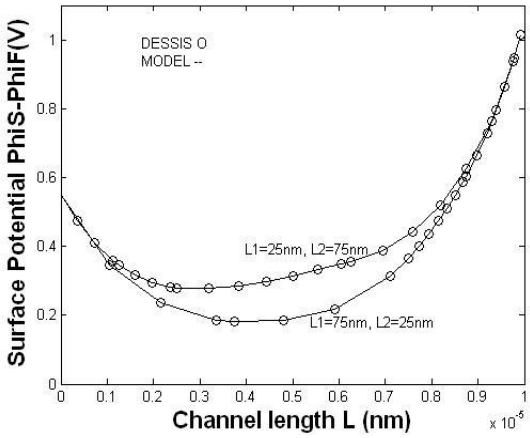


Figure. 21 The SHDMG potential profiles for two sets of gate materials L_1=25 nm and L_2=75 nm andL_1=75 nm and L_2=25 nm.

IV. CONCLUSION

An analytical subthreshold surface potential model for Double-Pocket Dual Material and Single-Pocket Dual Material Gate MOSFETs have been proposed in this paper that accounts for its dependence on varying depth along the channel depletion layer due to the source and the drain junctions. The models can predict the surface potential profile accurately for a wide variation of the device parameters such as the substrate concentration,the channel length, gate metals with different work functions and also for the different biasing conditions. Our model is verified against the 2D device simulator DESSIS. A very good aggrement of our model with results from DESSIS is obtained. The dependence of the surface potential on the junction depth is accommodated as per the scaling guide lines of ITRS roadmap.

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