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A FIRST ORDER ALL PASS FILTER AND ITS APPLICATION IN A QUADRATURE OSCILLATOR

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ABSTRACT

This paper presents an all pass voltage mode filter based on recently proposed active building block namely differential voltage current conveyor transconductance amplifier (DVCCTA). The proposed configuration uses single active and two grounded passive components which makes it suitable for IC implementation. Its input impedance is high and output impedance is low, hence suitable for cascading. The practical design problems due to non-idealities of DVCCTA have also been addressed. Moreover, as an application, a quadrature oscillator is designed using the proposed all pass circuit which provides both voltage and current outputs. SPICE simulation using 0.25 µm TSMC CMOS technology parameters are included to show the workability.

Keywords: All pass filter, Differential voltage current conveyor transconductance amplifier, Quadrature oscillator.

I. INTRODUCTION

In the field of electrical engineering, an analog filter is an important building block widely used for continuous-time signal processing. The magnitude characteristics play an important role in filter applications pertaining to voice or audio frequency range due to insensitivity of ear to change in phase. However, in video signal transmission, phase characteristics dominate. All pass filters are widely used for shifting the phase of the input signal while keeping the amplitude constant over the desired range of frequency. All-pass filters have been used in the realization of dual element frequency controlled oscillator with certain benefits in harmonic rejection and quadrature property [1], multiphase oscillators [2] and high quality frequency selective filters [3].

This paper presents a voltage mode first order all pass filter and its application as quadrature oscillator based on recently proposed active building block namely differential voltage current conveyor transconductance amplifier (DVCCTA) [4]. DVCCTA has differential voltage current conveyor (DVCC) [5] as input block and is followed by transconductance amplifier (TA). The DVCCTA has all the good properties of current conveyor transconductance amplifier (CCTA) [6, 7], current controlled current conveyor transconductance amplifier (CCCCTA) [8], and also all the versatile and special properties of DVCC such as easy implementation of differential and floating input circuits [5, 9, 10, 11]. The proposed circuits have been implemented using 0.25 µm TSMC CMOS technology and are validated through SPICE simulations for their functionality.

II. CIRCUIT DESCRIPTION

The circuit symbol of DVCCTA is shown in Fig. 1. The port relationships of the DVCCTA as shown in Fig. 1 can be characterized by the following matrix:

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ V_X \\ I_{Z+} \\ I_{Z-} \\ I_{O-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & -g_m & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ I_X \\ V_{Z+} \\ V_{Z-} \\ V_{O-} \end{bmatrix} \tag{1}$$

where g_m is transconductance of the DVCCTA. The CMOS based internal structure of DVCCTA is depicted in Fig. 2. It consists of a differential amplifier as input, a number of current mirrors [4], followed at the output by a transconductance amplifier. The value of g_m is given as $\sqrt{2\mu C_{ox}(W/L)_{21,22} I_0}$ which can be adjusted by bias current I_0.

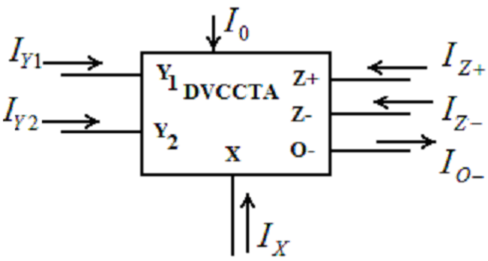

Figure 1. Circuit symbol of DVCCTA

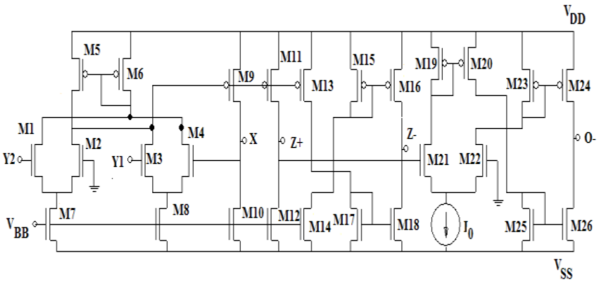

Figure 2. Internal structure of DVCCTA using CMOS

The proposed first order all pass filter (APF) based on DVCCTA is shown in Fig. 3. It uses a single DVCCTA, and one grounded resistance and capacitance each.

The transfer function of the proposed circuit is expressed as

$$\frac{V_{out}}{V_{in}} = \frac{sC - g_m}{sC - g_m + 1/R} \qquad (2)$$

With $g_m = 1/2R$, it reduces to the form of all pass filter as

$$\frac{V_{out}}{V_{in}} = \frac{sC - 1/2R}{sC + 1/2R} \qquad (3)$$

and its phase is expressed as

$$\varphi(\omega) = 180° - 2\arctan(2\omega CR) \qquad (4)$$

The resistance being a grounded one may easily be implemented as a variable active resistance using only two MOS [10]. Hence, the phase of the proposed filter can be tuned electronically by simultaneous adjustment of g_m by bias current (I_0) and R such that the product $g_m R$ remains constant. Already a number of attractive all pass filters based on DVCC are available in the literature [12 – 17]. Although, the proposed configuration based on DVCCTA needs matching constraint in contrast to [12,14,17] and difficult tunable property compared to [12], it has the following favorable features: i) uses single active block in contrast to multiple active blocks in [12– 17], (ii) uses less number of passive elements than [13, 15, 16], (iii) uses all grounded passive elements as opposed to [14, 16], and (iv) its input impedance is high and output impedance is low, hence suitable for cascading in contrast to [12 – 16].

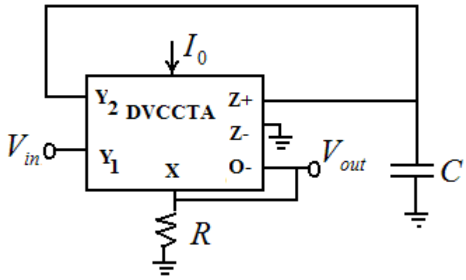

Figure 3 Proposed voltage mode all pass filter

III. QUADRATURE OSCILLATOR

The all pass filter of Fig. 3 may be used as quadrature oscillator when connected with an integrator in a closed loop. Fig. 4 shows the desired connections. The analysis of the circuit of Fig. 4 gives the following characteristic equation (with $g_{m1} = 1/2R_1$)

$$s^2C^2R_2 + sC(R_2 g_{m1} - 1) + g_{m1} = 0 \qquad (5)$$

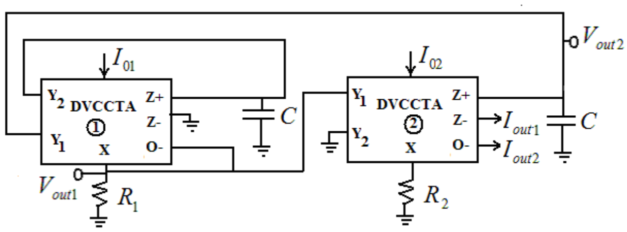

Figure 4 Proposed voltage mode and current mode quadrature oscillator

The condition and frequency of oscillation are expressed as

$$\text{CO: } R_2 g_{m1} = 1 \qquad (6)$$

$$\text{FO: } \omega_0 = \frac{1}{C}\sqrt{\frac{g_{m1}}{R_2}} \qquad (7)$$

The relationship between two output voltages V_{out1} and V_{out2} is obtained as

$$V_{out1} = sCR_2 V_{out2} \qquad (8)$$

and that between I_{out1} and I_{out2} as

$$I_{out2} = \frac{g_{m2}}{sC} I_{out1} \tag{9}$$

Thus both the voltage and current outputs give quadrature relationship. It may also be noted in (9) that the amplitude of I_{out2} may be modulated by changing the value of g_{m2} via the bias current (I_{02}) of 2nd DVCCTA

IV. INFLUENCE OF NON-IDEALITIES

The frequency performance of the filter circuit may deviate from the ideal one due to non-idealities of DVCCTAs. The non-idealities effects may be categorized in two groups. The first comes from frequency dependence of internal current and voltage transfers of DVCCTA. The modified port relationships may be written in matrix form as

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ V_X \\ I_{Z+} \\ I_{Z-} \\ I_{O-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ \beta_1 & -\beta_2 & R_X & 0 & 0 & 0 \\ 0 & 0 & \alpha_+ & 0 & 0 & 0 \\ 0 & 0 & -\alpha_- & 0 & 0 & 0 \\ 0 & 0 & 0 & -\gamma g_m & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ I_X \\ V_{Z+} \\ V_{Z-} \\ V_{O-} \end{bmatrix} \tag{10}$$

Where the coefficients $\beta_1 = 1 - \varepsilon_{v1}$ and $\beta_2 = 1 - \varepsilon_{v2}$. The ε_{v1} and ε_{v2} denote voltage tracking errors from Y1 and Y2 terminals to X terminal respectively. The coefficients $\alpha_+ = 1 - \varepsilon_{i+}$ and $\alpha_- = 1 - \varepsilon_{i-}$. The ε_{i+} and ε_{i-} denote current tracking errors from X to Z+ and Z- terminals respectively. The coefficient γ denotes current gain from Z+ terminal to O- terminal. The transfer functions represented in **(2)** is modifies as

$$\left.\frac{V_{out}}{V_{in}}\right|_{NI} = \frac{sC - \alpha\gamma g_m}{sC + (\alpha\beta_2 / R) - \alpha\gamma g_m} \tag{11}$$

where NI stands for non-ideal. With $\gamma g_m = \beta_2 / 2R$, it reduces to the form of all pass filter as

$$\left.\frac{V_{out}}{V_{in}}\right|_{NI} = \frac{sC - \beta_2 / 2R}{sC + \beta_2 / 2R} \tag{12}$$

and its phase is expressed as

$$\varphi(\omega) = 180° - 2\arctan(2\omega CR / \beta_2) \tag{13}$$

The analysis of quadrature oscillator, including non-idealities, results in the characteristic equation as

$$s^2C^2R_2 + sC(\alpha_1\beta_{21}R_2G - \alpha_1\gamma_1R_2g_{m1} - \alpha_2\beta_{12})$$

$$+\alpha_1\alpha_2\beta_{12}\gamma_1 g_{m1} = 0 \quad (8) \tag{14}$$

where α_i, β_{1i}, β_{2i}, γ_i (i=1, 2) are transfer coefficients for ith DVCCTA. The condition and frequency of oscillation may be computed as

$$\text{CO: } \alpha_1\gamma_1 R_2 g_{m1} = \alpha_2\beta_{12} \text{ as } \gamma_1 g_{m1} = \beta_{21}G/2 \tag{15}$$

$$\text{FO: } \omega_0 = \frac{1}{C}\sqrt{\frac{\alpha_1\alpha_2\beta_{12}\gamma_1 g_{m1}}{R_2}} \tag{16}$$

Equations (12), (13), (15) and (16) clearly indicate that the non-unity voltage and current transfer functions of DVCCTA affect the overall filter response, condition and frequency of oscillation for quadrature oscillator. The current and voltage transfer functions apart from having non-unity values, also have poles at high frequencies. However, the maximum frequency of operation will be limited by poles of voltage (f_β) and current (f_α, f_γ) transfers which are simulated to be 244 MHz, 885MHz and 606MHz respectively for the DVCCTA of Fig. 2. The effect can however be ignored if the operating frequencies are chosen sufficiently smaller than voltage and current transfer pole frequencies of the DVCCTA.

The second group of non-idealities comes from parasites of DVCCTA comprising of resistances and capacitances connected in parallel at terminals Y1, Y2, Z and O- (i.e. $R_{Y1}, C_{Y1}, R_{Y2}, C_{Y2}, R_Z, C_Z, R_{O-}, C_{O-}$) and an intrinsic resistance R_X at terminal X. The effects of these parasites on filter response depend strongly on circuit topology. The APF topology of Fig. 3, in the presence of these parasites, modifies to Fig. 5 where $C_{eq} = C // C_{Y2} // C_Z$, $C_{1p} = C_{O-}$, $G_{eq} = 1/(R_{O-} // R)$ and $G_{1p} = 1/(R_{Y2} // R_Z)$.

Considering the parasites outlined above, (2) modifies to

$$\left.\frac{V_{out}}{V_{in}}\right|_{NI} = \frac{sC_{eq} - g_m - G_{1p}}{\Delta} \tag{17}$$

where

$$\begin{aligned}\Delta &= sC_{eq} - g_m - G_{1p} \\ &\quad + G_{eq}(1 + sC_{1p}/G_{eq})(1 + R_XG_{1p} + sC_{eq}R_X) \\ &\approx sC_{eq} + G_{eq} - g_m - G_{1p} \\ &\quad \text{for } R_X << R_{Y2} // R_Z \text{ and} \\ &\quad \omega << \min(1/(R_XC_{eq}), (G_{eq}/C_{O-}))\end{aligned} \tag{18}$$

The condition for APF and phase response modify to

$$g_m = (G_{eq}/2) - G_{1p} \tag{19}$$

and

$$\varphi(\omega) = 180^\circ - 2\arctan(2\omega C / G_{eq}) \qquad (20)$$

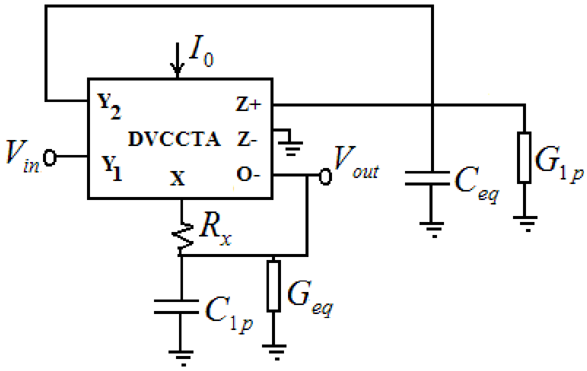

Figure 5 Proposed all pass filter with parasitic components

It may be noted in (18) that the maximum operating frequency will be influenced by parasitic resistance at X port and capacitance at O- port. The parasitic capacitance at Y2 and Z port may be accommodated in external capacitor. The parasitic resistances and capacitances for DVCCTA are simulated to be $R_X = 23\Omega$, $R_Y = very\,high$, $C_Y = 20\,fF$, $R_Z = 215k\Omega$, $C_Z = 0.8\,pF$, $R_{O-} = 193k\Omega$, $C_{O-} = 9\,fF$. It may be noted that the condition $R_X << R_{Y2} // R_Z$ is satisfied and by selecting $R >> R_X$ and $C >> C_{O-}$, the effect of parasites may practically be ignored.

The topology of quadrature oscillator including parasites of DVCCTA is shown in Fig. 6. Taking (19) into consideration, the analysis of this topology results in the following characteristic equation.

$$s^2 C_{eq1} C_{eq2} + sC_{eq1}(G_{2p} - G_{eq2}) + sC_{eq2}(G_{eq1}/2)$$
$$+ (G_{eq1}/2)(G_{eq2} + G_{2p}) = 0 \qquad (21)$$

where $C_{eq1} = C // C_{Y21} // C_{Z1}, C_{eq2} = C // C_{Y11} // C_{Z2}$, $C_{1p} = C_{O-1} // C_{Y12}, G_{eq1} = 1/(R_{O-1} // R_1 // R_{Y12})$, $G_{eq2} = 1/(R_{X2} + R_2)$, $G_{1p} = 1/(R_{Y21} // R_{Z1})$ and $G_{2p} = 1/(R_{Y11} // R_{Z2})$.

The condition and frequency of oscillation in presence of parasites may be computed as

$$\text{CO: } G_{eq2} - G_{2p} = G_{eq1}/2, \quad C_{eq1} = C_{eq2} \qquad (22)$$

$$\text{FO: } \omega_0 = \sqrt{\frac{G_{eq1}(G_{eq2} + G_{2p})}{2C_{eq1}C_{eq2}}} \qquad (23)$$

It may be noted that the values of C_{eq1} and C_{eq2} are equal. The value of resistor R_2 may be pre-adjusted to accommodate parasitic R_{X2}. The effect of parasitic resistors may be ignored if the values of resistors R_1 and R_2 are selected much higher then the R_{X1} and R_{X2}.

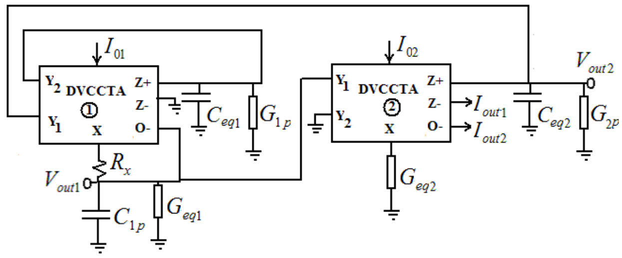

Figure 6 Proposed quadrature oscillator with parasitic components

V. SIMULATION RESULTS

To validate the theoretical analysis, the circuit of Fig. 3 is designed for a phase shift of 90° at f_0 = 1.59 MHz. The model parameters of TSMC 0.25µm CMOS process and supply voltages of $V_{DD} = -V_{SS}$ = 1.25V and V_{BB}= - 0.8V are used. The aspect ratio of various transistors as specified in Table 1 are taken from [17] for the DVCC part of DVCCTA circuit. The bias current I_0 of 100 µA and dimensions of M_{21} and M_{22} are selected so as to provide g_m value of 0.001mho. The designed values of C and R are respectively 100 pF and 0.5kΩ. The simulation and theoretical results for magnitude and phase responses of all pass filter are shown in Fig. 7, which show close agreement with each other. The transient response of the proposed all pass filter, as shown in Fig. 8, for a 1.59 MHz sinusoidal signal clearly depicts a phase difference of 90° between input and output. The relation between input and output magnitudes is shown in Fig. 9.

Table 1.Aspect ratio of various transistors

M7,M8	27.25/0.5
M9,M11,M13,M15,M16	8.5/0.5
M10,M12,M14,M17,M18	44/0.5
M19,M20, M23 – M26	5/0.5
M21, M22	27/0.5

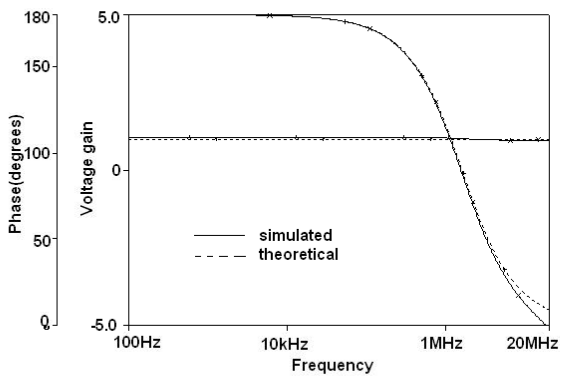

Figure 7 Magnitude and phase response of the proposed voltage mode all pass filter

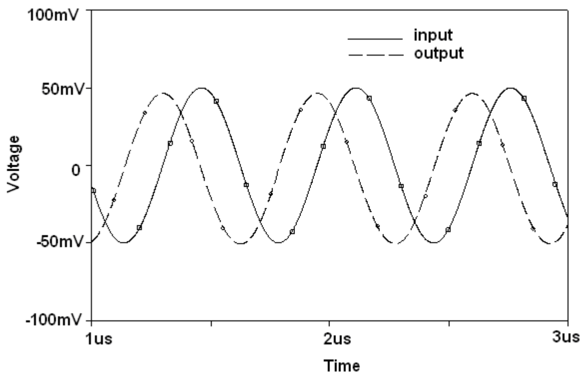

Figure 8 Transient response of the filter with sinusoidal input at 1.59MHz

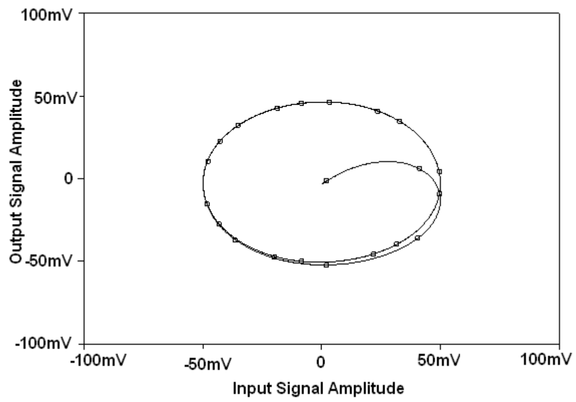

Figure 9 Relation between magnitudes of input and output

The proposed all pass filter circuit is also tested against temperature variations through simulations. The results are depicted in Fig 10. The performance analysis of the response shows that the variation in gain at 100 Hz is significant (1.07 at 27˚C and 0.688 at 125˚C) whereas almost negligible deviation in the pole frequency is observed in the phase response.

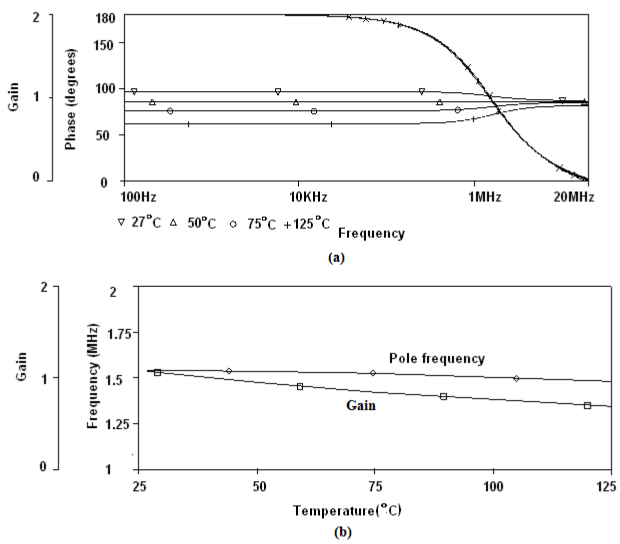

Figure 10 Effect of temperature on all pass response (a) frequency vs phase and gain at different temperatures (b) temperature vs gain at 100 Hz and pole frequency.

To demonstrate the functionality of quadrature oscillator, an oscillator is designed for 1.59 MHz frequency. The various component values are: R_1 = 0.5 kΩ, R_2 = 1 kΩ, C = 100 pF and I_{01} = I_{02} = 100 μA. The simulated results for voltage and current outputs of quadrature oscillator are shown in Fig. 11. The ability of obtaining the modulated output current I_{out2} by varying g_{m2} through bias current I_{02} is depicted in Fig. 12.

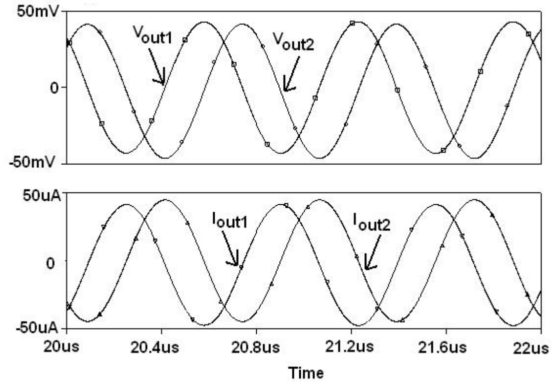

Figure 11 Simulated output voltage and current waveforms at 1.59MHz

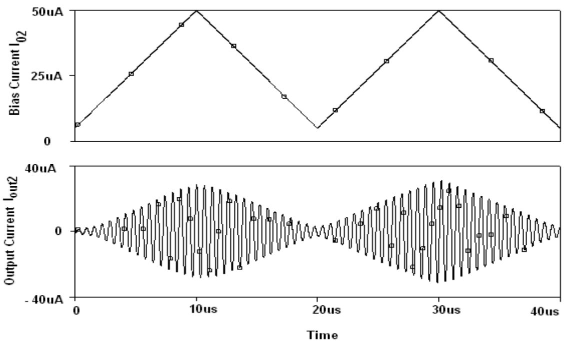

Figure 12 The amplitude modulated waveform for I_{out2} for various values of I_{02}

VI. CONCLUSION

A new VM first order all pass filter configuration has been presented in this paper that uses a single DVCCTA, one grounded capacitor and one grounded resistance. The topology is suitable for cascading as it possesses high input and low output impedances. As an application of the proposed filter, a quadrature oscillator is constructed which can provide simultaneously both voltage mode and current mode outputs from the same topology. The proposed circuits have been implemented using 0.25 μm TSMC CMOS technology and are validated through SPICE simulations for their functionality.

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