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PRE-SETTABLE SEQUENTIAL CIRCUITS DESIGN USING SINGLE-CLOCKED ENERGY EFFICIENT ADIABATIC LOGIC

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Abstract
In this paper, the design of pre-settable adiabatic flip-flops and sequential circuits based on the newly proposed Energy efficient adiabatic Logic (EEAL) is presented. EEAL is based on differential cascode voltage swing (DCVS) logic, uses only a single sinusoidal source as supply-clock. This not only ensures lower energy dissipation, but also simplifies the clock design which would be otherwise more complicated due to the signal synchronization requirement. An adiabatic asynchronous sequential circuit with a reset line has been implemented using EEAL style in a TSMC 0.18 μm CMOS technology. CADENCE simulation shows that EEAL based sequential circuit consumes only 24%-36% of total energy consumed by others imperative logic styles. Layouts of the proposed EEAL based D and JK Flip-flops are given to estimate the silicon area clearly.

Keywords: Adiabatic logic, Pre-settable flip-flops, single-clock, energy efficient, adiabatic counter

I. INTRODUCTION

As the transistor count per chip increases rapidly in the system-on-chip (SoC) era, significant reduction in power overhead in dynamic switching and leakage is of particular importance. Adiabatic logic style has emerged as a promising approach to achieve ultra-low power without sacrificing noise immunity and driving ability.

A plethora of adiabatic logic styles [1]-[10], which have been proposed over the past decade depend on multiphase clocking schemes. The problems with multiphase clocking [2]-[4], [6], [7], [11] include complicated clock tree design with clock skew, and increased energy dissipation with power clock generators [2], [3], [6], [8], [11]. To ensure signals that originate from different clock phases to be synchronized, insertion of data buffers is required which cause extra power dissipation and area cost [1], [9]. In order to make these adiabatic logic circuits more feasible and practical in VLSI applications, single-clock operation of the circuits would be needed. Though few adiabatic logics including SCAL (Source coupled Adiabatic Logic) [1], SCALD (Source coupled Adiabatic Logic with diode) [2], CAL (Clocked Adiabatic Logic) [3], PAL (Pass Transistor Adiabatic Logic) [4] and QAPG (Quasi Adiabatic Pass gate Logic) [5] have been reported on single clock operation yet in practical cases they suffer in high frequency regime. Requirement of additional voltage and current sources increase the complexity in SCAL and SCALD [1], [2]. To ensure correct operation auxiliary clocks are required in CAL which deteriorates the energy efficiency. Cascaded PAL structure operates under complementary clocks and suffer from undesired capacitive couplings, since the output nodes are kept floating instead of zero. Higher silicon area imposes limitation on the QAPG operation. In this paper we proposed an energy efficient adiabatic logic (EEAL) based on DCVS network. EEAL operates under a single sinusoidal source. As a parallel path is always provided between the clock supply and output nodes, floating output problems can be eliminated completely which in turns enhances the energy efficiency.

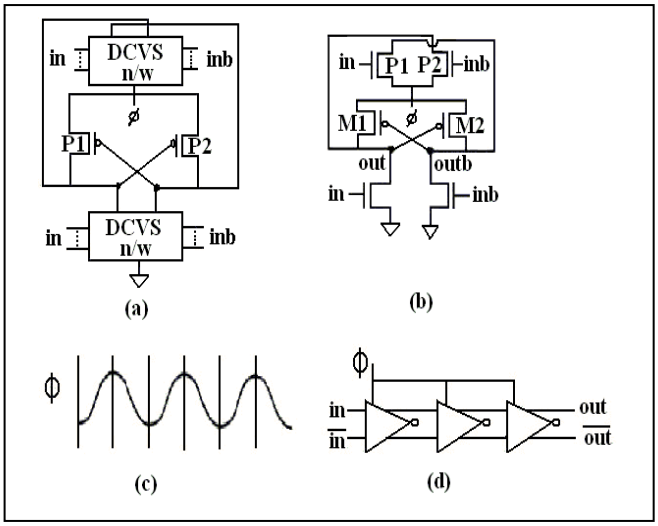

Figure 1. EEAL logic (a) Block diagram (b) Inverter/Buffer circuit (c) Power supply (d) Cascading of Inverter/Buffer circuits

Previously reported adiabatic logic styles focused mainly on combinational logic designs such as CLA, ALU, and processor [2], [7]-[9]. However, flip-flops and sequential circuits cannot be also neglected in digital systems, as we cannot build adiabatic sequential circuits by simply using

conventional method. In this paper, we focus on the design and analysis of adiabatic asynchronous sequential circuits based on the single phase EEAL. Extensive CADENCE simulations have done to show the workability of the proposed logic using 0.18µm CMOS technology in various frequency ranges.

The rest of the paper is organized as follows. Rudimentary operation of EEAL logic is discussed in section II. Section III describes the design and operation of sequential circuit such as D, JK, T flip-flops and adiabatic decimal up counter using EEAL. Experimental results and comparison of performance of EEAL with CAL, QAPG and static CMOS logic are also detailed in this section. Finally conclusions are given in section IV.

II. OPERATION OF EEAL

EEAL is a dual-rail adiabatic logic which consists of two DCVS network and a pair of cross-coupled PMOS devices in each stage, as illustrated by Figure 1(a). To ensure correct operation a sinusoidal ac supply, shown in Figure 1 (c) is used. Figure 1 (b) shows the EEAL buffer/Inverter circuit which is based on Figure 1 (a).

As far as operation is concerned assuming "out" and "outb" are initially low and φ ramps up from logic 0("0") to logic 1("V_{DD}") state. If now "in" = "0"and "inb"= "1"; N1, P1 are turned off and N2, M1 and P2 are turned ON. The "out" node is then charged by following φ closely through the parallel combination of P2 and M1, whereas "outb" node is kept at ground potential, as N2 is "On". When φ swings from "V_{DD}" to ground, "out" node is discharged through the same charging path and "outb" is kept at same ground potential. Resultantly we get full swing in "out" node and ground potential at "outb" node. So floating output problem can be eliminated which in turn increases the energy efficiencies of EEAL based circuits.

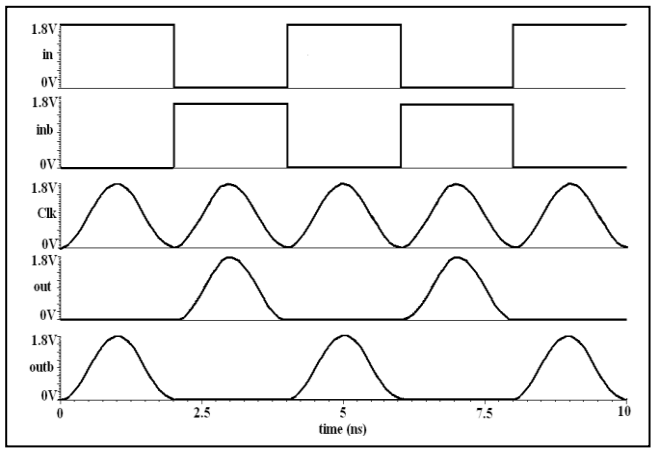

Figure 2. Output waveforms of EEAL Inverter/Buffer circuit at 100MHz with a load of 25fF at the output nodes

TSMC 0.18µm CMOS process is used to simulate the proposed EEAL Inverter/Buffer circuit. The CADENCE simulation waveforms of the EEAL Inverter/Buffer are shown in Figure 2. These simulation results were obtained when a periodic sequence "1010 ..." was applied at the input of Figure 1 (b). The frequency of the power-clock is 100MHz**,** and its peak voltage 1.8V**.** W/L of the cross coupled PMOS (M1 and M2) is taken with 12λ/2λ, and the other NMOS transistors are taken with 6λ/2λ where λ=0.9µm.

Energy dissipation of the EEAL circuits includes mainly full-adiabatic energy loss on output nodes. In EEAL, as floating problem is solved by providing parallel paths between output nodes and supply clock, energy loss on internal nodes due to leakage currents become negligible. Moreover in parallel paths either PMOS or NMOS any one or both transistors are turned "ON" always. So the voltage drop across the path becomes very small (ΔV≈ 0) which reduces the threshold loss also. Thus the non-adiabatic loss is minimized significantly. The energy dissipation in charging process of the EEAL inverter/buffer can be expressed as:

$$E = \{(RC_L)/T\} (C_L V_{DD} \quad + ½ C_L(\Delta V)^2 \qquad (1)$$

Hence R is the turn-on resistance of the parallel path, C_L is the output load capacitances and T is the charging time. $½C_L(\Delta V)^2$ shows the threshold loss [4], [9], [11]. Though this loss is negligibly small yet it is included in the above equation to make the power consumption more realistic. In EEAL as charging and discharging processes consume almost similar amount of energy, total energy dissipation for a complete cycle can be expressed as:

$$E = 2\{(RC_L)/T\} (C_L V_{DD})^2 + C_L (\Delta V)^2 \qquad (2)$$

The above calculation implies that we may dramatically reduce the power dissipation by somehow prolonging T. Hence during charging and discharging, PMOS/NMOS transistors are operated in triode region as very small voltage drop occurs between supply clock and output nodes. So the turn-on resistance of the charging or discharging path consists of parallel combination of PMOS/NMOS transistors can be expressed as:

$$R=\{\mu_n C_{ox}(W/L)_n(½V_{DD}-V_{tn})+\mu_p C_{ox}(W/L)_p(½V_{DD}-V_{tp})\} \qquad (3)$$

where μ_n and μ_p are the mobility of PMOS and NMOS; V_{tn} and $|V_{tp}|$ are the threshold voltages of PMOS and NMOS respectively; all the other terms have the usual meaning. For 0.18µm CMOS process, considering V_{DD}=1.8V and $(\quad)_p=2(\quad)_n$, the above expression gives R=1.02KΩ. Similarly the load capacitances (C_L) associated with PMOS/NMOS transistors, operating in triode region can be expressed by:

$$C = W (½L+\Delta L) C_{ox} + C_J \quad (4)$$

where ΔL is the overlap capacitances and C_{ox} is the gate oxide capacitances per unit area. In 0.18µm CMOS process, C_{ox} is approximately 8.6fF/µm^2. Capacitance C_J is due to the junction between the source/drain diffusion and the bulk.

Comparing Figure 1 (b) with first order RC network signal propagation delay can be expressed as:

$$\tau_{RC} = (\ln 2)\, RC_L \quad (5)$$

In 0.18µm CMOS process considering 10fF output load, RC time delay (τ_{RC}) of EEAL Inverter/buffer circuit becomes almost 7.04 ps. Due to parallel resistive path signal propagation in EEAL will be very faster compared to other imperative logic styles.

III. ADIABATIC PRE-SETTABLE SEQUENTIAL CIRCUIT DESIGN

In this section, we first describe the EEAL gates, and then we present the design of adiabatic flip-flops and sequential circuits using EEAL gates.

III.1 EEAL Complex Gate Design

Complex EEAL gate can be implemented easily by using the general structure shown in Figure 1 (a). In Figure 1 (a), replacing DCVS networks by the structures shown in Figure 3, we can implement 2 i/p AND, OR, XOR and 2-1 MUX. Thus complex gate designs by EEAL logic become simple and modular.

III.2 EEAL Pre-Settable Flip-Flop design

A few adiabatic logic architectures have been presented for low power sequential circuit design [12]-[15] with a single or multiphase clock scheme. Implementation of complex control schemes, distribution of multiple clock phases, management of data dependent clock capacitance fluctuations make the multiphase clocking schemes sensitive to clock skew. In previously proposed transistor based adiabatic circuits; a complicated clocking rule must be followed to form a chain of cascaded stages. These all impose limitations on sequential circuit design by multiphase clock based adiabatic logics. Hence we implement the adiabatic sequential circuit by EEAL logic which uses a single sinusoidal clock source. Moreover sinusoidal power-clocks have more practical significance because it can be easily produced using simple *LC* circuits. This not only ensures low energy consumption yet enjoys minimal control overhead also.

To establish a simple sequential circuit, like D flip-flop, two cascaded inverter stages or a single buffer stage driven by a single sinusoidal clock are required. According to this method, the adiabatic *D* flip-flop using the EEAL circuits is shown in Figure 4(a). The energy loss of a D flip-flop can be expressed as,

$$E = 2\{R (C_1+C_2)/T\} (C_L V_{DD} \quad + (C_1+C_2)(\Delta V \quad (6)$$

where C1 and C2 are the output load capacitance of two successive inverter stages. Assuming that the present and next stage of adiabatic D flip-flop is Q and Q*. In case of T and JK flip-flop, output can be written as Q* = TQ'+QT' and Q* = JQ'+ KQ. So the T and JK flip-flops can be realized by

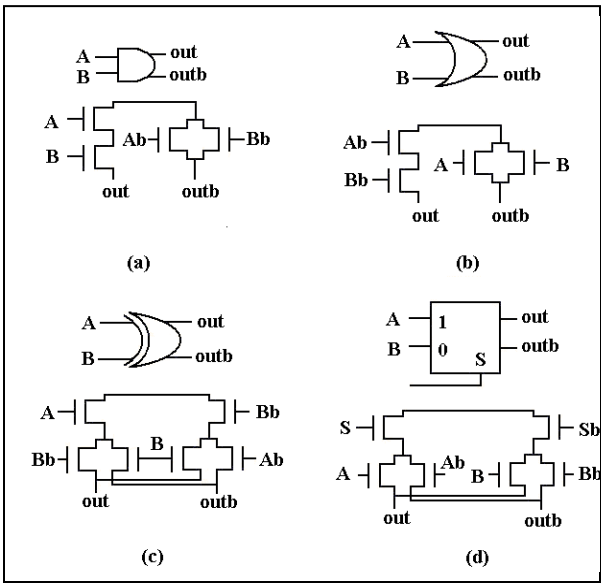

Figure 3. DCVS network of EEAL Gates (a) AND/NAND (b) OR/NOR (c) XOR/XNOR and (d) 2-1 MUX

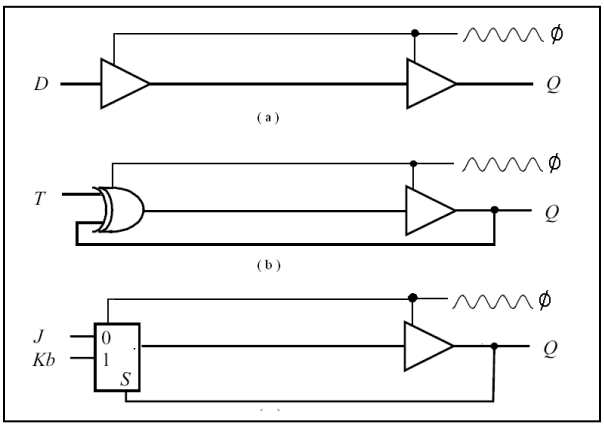

Figure 4. EEAL sequential circuits (a) D Flip-flop (b) T Flip-flop (c) JK Flip-flop

using the XOR and multiplexer to replace the first-EEAL buffer stage in the adiabatic *D* flip-flop. The *T* and *JK* flip-flops using two-stage EEAL are shown in Figure 4(b) and Figure 4 (c), respectively.

Adiabatic flip-flops with a reset line are more universal and suitable for the design of adiabatic sequential circuits. To implement the pre-settable adiabatic flip-flops, second stage of EEAL flip-flops will be replaced by the 2-1 multiplexer. Figure 5 shows the pre-settable D flip-flop and T flip-flop.

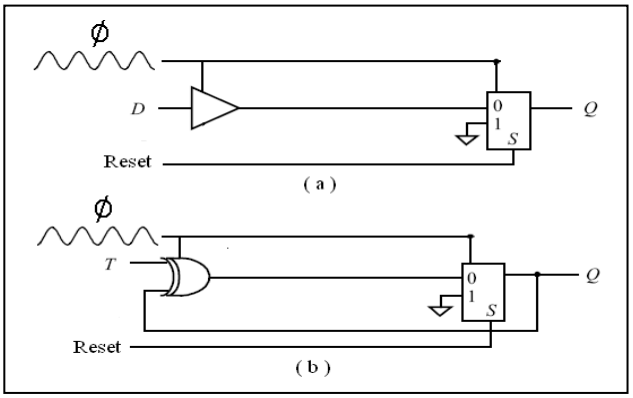

Figure 5 Pre-settable adiabatic flip-flops (a) D flip-flop (b) T flip-flop

Output waveform of EEAL based pre-settable D flip-flop are shown in Figure 6. Figure 7 shows that EEAL D flip-flop performs better than the other imperative adiabatic logic styles. At 100MHz frequency, EEAL based D flip-flop consumes only 19.12%, 29%, 40% and 47% of total power consumed by conventional CMOS, 2N2N2P, CAL and CTGAL respectively. Simulated waveform of pre-settable T flip-flop is also shown in Figure 8.

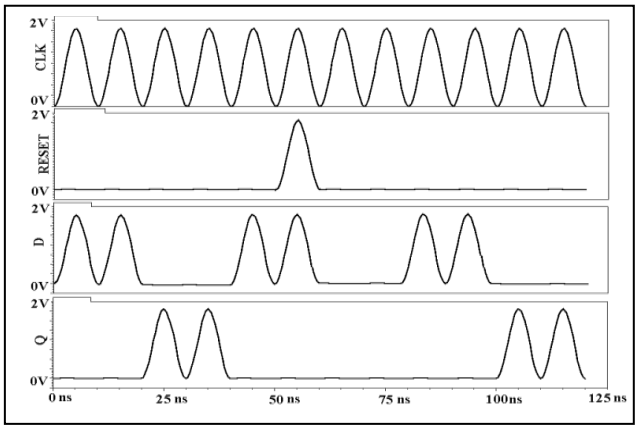

Figure 6 Output waveforms of EEAL pre-settable D flip-flop circuit at 100MHz with a load of 25fF at the output nodes

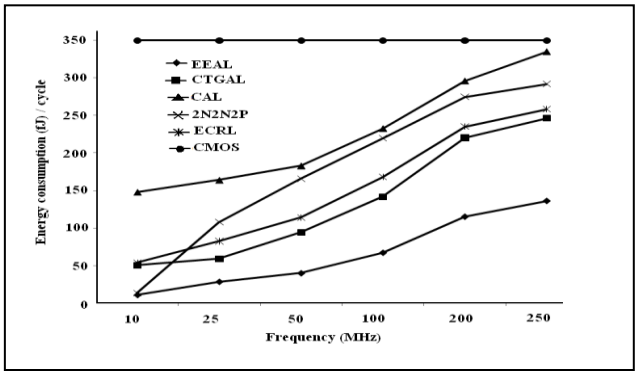

Figure 7. Comparison of energy consumption per cycle of EEAL, ECRL [7], CTGAL [10], CAL, 2N2N2P [6] and static CMOS based D Flip-Flop

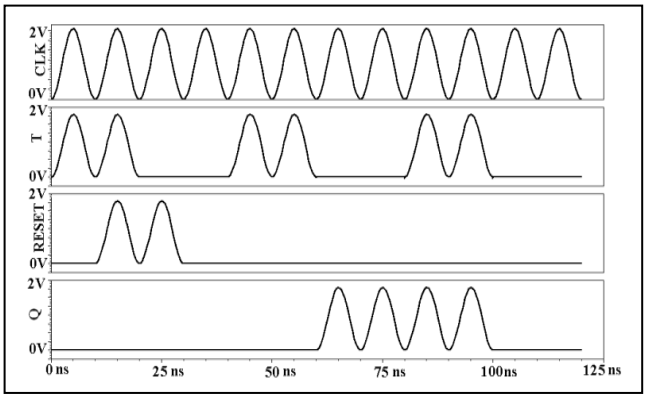

Figure 8. Output waveforms of EEAL JK flip-flop circuit at 100MHz with a load of 25fF at the output nodes

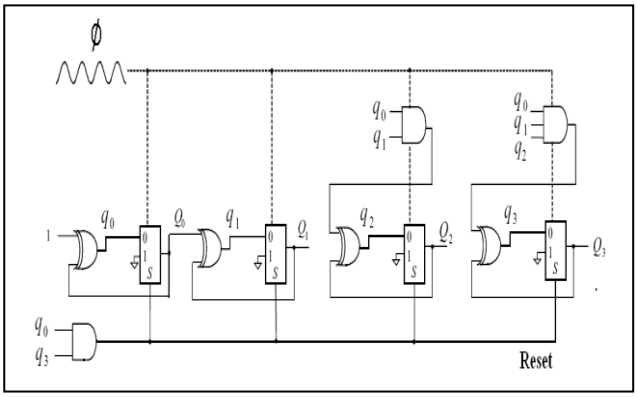

Figure 9. Schematics of decimal up counter based on EEAL logic

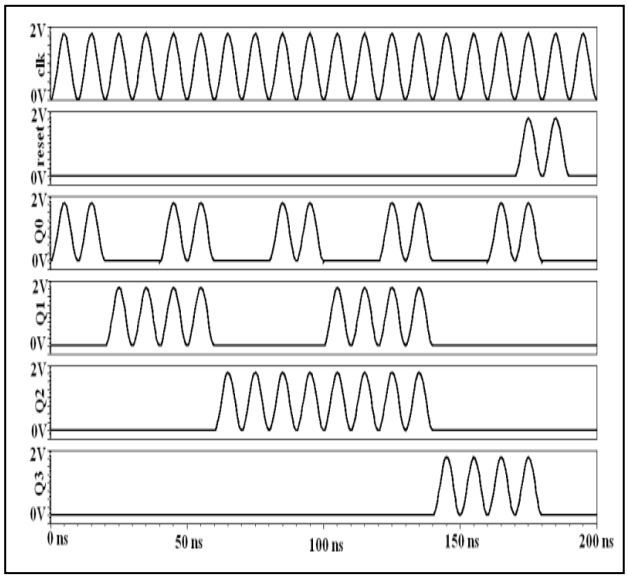

Figure 10. Output waveforms of EEAL Inverter/Buffer circuit at 100MHz with a load of 25fF at the output nodes

III.3 EEAL Pre-Settable Flip-Flop design

Complex sequential circuits can be realized using the schematic of a BCD code up counter which is implemented by pre-settable flip-flops and EEAL gates. The proposed pre-settable flip-flops and EEAL gates. Figure 9 shows transition function of each flip-flop can be expressed as $Q0^* = Q_0'$, $Q_1^* = (Q_0 \oplus Q_1)\, Q_3'$, $Q_2^* = (Q_0Q_1) \oplus Q_2$, $Q_3^* = ((Q_1Q_2)Q_0 + Q_3Q_0')$. We can also realize the other counter by modifying the 'reset' signal in Figure 9. Simulated waveforms of EEAL based decimal up counter are shown in Figure 10. Therefore, the proposed pre-settable adiabatic flip-flops are more universal and suitable for the design of adiabatic counters. In Figure 11 CADENCE simulation shows that EEAL based decimal up counter consumes only 24.5%, 35.5% and 26% of total power consumed by conventional CMOS, 2N2N2P and CAL. Layouts of D and JK Flip-flops are shown in Figure 12 to estimate the silicon area clearly. In case of adiabatic logic style, as we are getting complementary output simultaneously, the transistor overheads and finally silicon area becomes larger. Still this complementary logic design becomes efficacious in implementing the complex circuits like multiplier, complex adder etc.

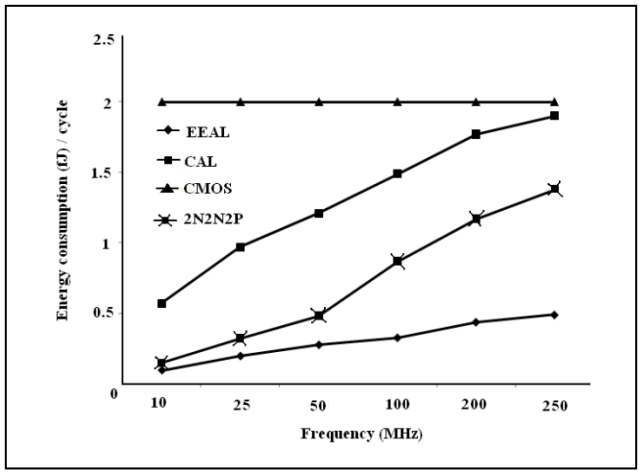

Figure 11. Comparison of energy consumption per cycle of EEAL, CAL, 2N2N2P and conventional CMOS logic based decimal up counter

IV. CONCLUSION

This paper proposes a single clock based energy efficient adiabatic logic. Non-adiabatic loss can be minimized significantly by eliminating floating output problem. This logic is also faster compared to other imperative logic styles as parallel path is provided between supply clock and output nodes. EEAL based pre-settable adiabatic flip-flops and decimal up counter are also implemented. CADENCE simulation shows the high energy efficiencies of EEAL logic. Both simulation and measurement results verify the functionality of such logic, making it suitable for implementing energy-aware and performance-efficient sequential circuit.

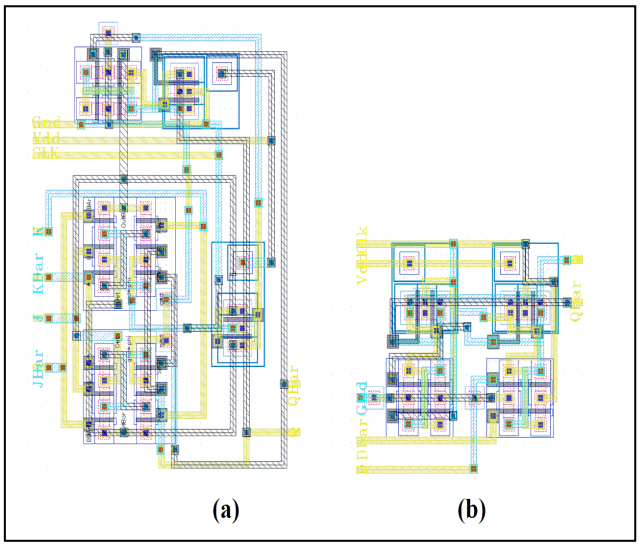

Figure 12. Layout of EEAL based (a) JK FLIP-FLOP and (b) D FLIP-FLOP

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