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DEPENDENCE OF DC AND SMALL-SIGNAL PROPERTIES OF DOUBLE DRIFT REGION SILICON IMPATT DEVICE ON JUNCTION TEMPERATURE

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Abstract:
Effect of junction temperature on the DC and high-frequency properties of W-band double drift (DDR) Silicon IMPATT device is investigated in this paper. A double iterative computer method based on drift diffusion model is used to simulate the device designed to operate at W-band and different junction temperatures. Results show that the peak operating frequency of the device decreases from *135 GHz* to *93 GHz*, while the RF power output increases from *517 mW* to *637 mW* when the junction temperature rises from *300 K* to *500 K*.

Keywords: Admittance characteristic, IMPATT device, Junction temperature, Negative resistance.

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I. INTRODUCTION

The rapid development of Silicon technology in the decade of seventies has made possible the practical realization of Silicon based single drift (SDR) and double drifts (DDR) IMPATT devices capable of providing RF output power of the order of several watts at microwave and millimeter-wave frequency bands [1-4]. The efficiency of the DDR Silicon IMPATT diode is relatively low, typically *10%* at W-band. Therefore a large fraction of the DC power is dissipated as heat in the high-field region. This causes a rise of junction temperature above ambient and consequently the output power from the device is limited by the rate at which heat can be extracted from the device. The amount of DC power, P_{max} that can be dissipated is determined by the burn-out temperature, T_B and thermal resistance, R_{th}: $P_{max} = (T_B - T_0)/R_{th}$, where, T_0 is the temperature of the ambient. The thermal resistance is the temperature rise at the junction when one watt of power is dissipated. Properly designed heat sink (made of copper or type-IIA diamond) is essential to keep the junction temperature of the device below the burn out temperature [5-9]. The DC and high frequency performance of IMPATTs depends on the material parameters [10] of the base semiconductor such as carrier ionization rates; drift velocities etc. These parameters are strongly dependent on the junction temperature of the device. In the present paper the authors have carried out an investigation on the effect of junction temperature on the high frequency performance of W-band DDR Silicon IMPATT device operating at steady state continuous wave (CW) mode.

II. DESIGN AND SIMULATION

The frequency of operation of an IMPATT diode essentially depends on the transit time of charge carriers to cross the depletion layer of the diode. IMPATT diode having double drift p^+pnn^+ structure is first designed for operation at *94 GHz* window by using simulation technique and the transit time formula of Sze and Ryder [11] given by $W_{n,p} = 0.37\, v_{sn,sp} / f_d$; where $W_{n,p}$, $v_{sn,sp}$ and f_d are the total depletion layer width (*n* or *p*-side), saturation velocity of electrons/holes and design frequency respectively. The background doping (*n* and *p* region doping) is varied in the simulation program [12] so that the electric field just punches through the depletion layers ($W_{n,p}$) for a particular value of f_d and a particular bias current density J_0. Small-signal analysis [13] based on Gummel-Blue approach [14] is then carried out to obtain the conductance-susceptance or admittance characteristics of the diode. The peak optimum frequency (f_p) for maximum negative conductance can be determined from the admittance characteristics. If the magnitude of f_p differs very much from f_d, the value of J_0 is varied and the computer aided design is repeated until f_p is nearly equal to f_d. The bias current density is thus obtained for the design frequency under consideration. A DDR Silicon IMPATT device is designed and optimized for CW operation at W-band by following the above mentioned method. The design parameters (doping and structural parameters) of the device are listed in Table 1. The junction diameter of the mesa structure of the device is taken to be $D_j = 35\ \mu m$ for CW mode of operation [15].

TABLE 1 DESIGN PARAMETERS

DESIGN FREQUENCY, f_d (GHz)	n-EPITAXIAL LAYER THICKNESS, W_n (μm)	p-EPITAXIAL LAYER THICKNESS, W_p (μm)	n-EPITAXIAL LAYER DOPING, N_D ($\times 10^{23}\ m^{-3}$)	p-EPITAXIAL LAYER DOPING, N_A ($\times 10^{23}\ m^{-3}$)	SUBSTRATE LAYER DOPING, N_{Sub} ($\times 10^{26}\ m^{-3}$)	BIAS CURRENT DENSITY, J_0 ($\times 10^{8}\ Amp/m^2$)
94	0.320	0.300	1.650	1.800	1.000	3.2

III. MATERIAL PARAMETERS

III.1 Variation of Electron and Hole Ionization Rates with Electric Field and Temperature

The carrier ionization rates in Silicon at different temperatures were experimentally measured by Grant et al [16] in 1973 at both lower and higher field ranges The empirical relations which fit well with the experimental data of variations of electron and hole ionization rates with electric field and temperature are expressed as:

Within the lower field range $2.4\times10^7 - 5.3\times10^7$ V/m,

$$\alpha_n(\xi,T_j) = 6.2\times10^7\left[exp\left\{-\frac{\left(1.08\times10^8 + 1.3\times10^5(T_j-22)\right)}{\xi}\right\}\right] \quad (1)$$

$$\alpha_p(\xi,T_j) = 2.0\times10^8\left[exp\left\{-\frac{\left(1.97\times10^8 + 1.1\times10^5(T_j-22)\right)}{\xi}\right\}\right] \quad (2)$$

Within the higher field range $5.3\times10^7 - 7.7\times10^7$ V/m,

$$\alpha_n(\xi,T_j) = 5.0\times10^7\left[exp\left\{-\frac{\left(9.90\times10^7 + 1.3\times10^5(T_j-22)\right)}{\xi}\right\}\right] \quad (3)$$

$$\alpha_p(\xi,T_j) = 5.6\times10^7\left[exp\left\{-\frac{\left(1.32\times10^8 + 1.1\times10^5(T_j-22)\right)}{\xi}\right\}\right] \quad (4)$$

Where, ξ is the electric field and T_j is the temperature in ^0C.

III.2 Variation of Electron and Hole Drift Velocities with Electric Field and Temperature

The empirical relations for the electron and hole saturated drift velocities in Silicon with electric field and temperature can be expressed as [17],

$$v_{sn} = \frac{1.42\times10^7\times T^{-2.42}\times\xi}{\left(1+\left(\frac{\xi}{1.01\times T^{1.55}}\right)^{0.0257\times T^{0.66}}\right)\times\left(\frac{1}{0.0257\times T^{0.66}}\right)} \quad (5)$$

$$v_{sp} = \frac{1.31\times10^7\times T^{-2.20}\times\xi}{\left(1+\left(\frac{\xi}{1.24\times T^{1.68}}\right)^{0.4600\times T^{0.17}}\right)\times\left(\frac{1}{0.4600\times T^{0.17}}\right)} \quad (6)$$

Where, ξ is the electric field and T is the temperature in K.

III.3 Variation of Electron and Hole Mobilities with Temperature

Theoretical calculations reveal that the mobility in non-polar semiconductors, such as Silicon, is dominated by acoustic phonon interaction. Variation of electron and hole mobilities with temperature can be expressed as [18],

$$\mu_n = 0.1350\times\left(\frac{T}{300}\right)^{-2.42} \quad (7)$$

$$\mu_p = 0.0480\times\left(\frac{T}{300}\right)^{-2.20} \quad (8)$$

Where, T is the temperature in K. Using the above relations the material parameters like, carrier ionization rates,

saturated drift velocities and mobilities can be obtained at any temperature.

IV. RESULTS AND DISCUSSION

A double iterative DC and small-signal simulation method [12-13] based on Gummel-Blue approach [14] is used to obtain the DC and high frequency properties of the device designed to operate at W-band frequencies. The design parameters are listed in Table 1. The variations of material parameters with temperature (equations (1) to (8)) are incorporated in the DC and small-signal program to simulate the device at different junction temperatures from room temperature, *300 K* to near burnout temperature of Silicon, i.e. *500 K*. The electric field and normalized current density ($P(x) = (J_p(x) – J_n(x))/J_0$) profiles of the device at different junction temperatures are shown in Figure 1. It can be observed from the Figure 1 that everywhere in the depletion region of the device, the electric field increases as the junction temperature increases. This increment in electric field at each space point causes an increment in breakdown voltage of the device at higher junction temperatures as shown in Figure 2 [Since, $V_B = \int\xi(x)\,dx$; where the integration is carried out throughout the depletion region of the device]. Figure 1 shows that the $P(x)$-profiles smear out as the junction temperature of the device increases. The extension of avalanche zone, defined as the width of the depletion layer within which the current grows up to *95%* of its DC value (J_0). The slope of this profile in the high field region near the junction determines the rate of current growth and thereby the width of avalanche zone. The sharper the slope of this profile, the faster is the growth of the avalanche current and narrower the avalanche zone. Figure 1 reveals that the avalanche zone of device is wider at higher junction temperatures. This phenomenon leads to lower efficiency of the device at higher junction temperatures (Figure 2).

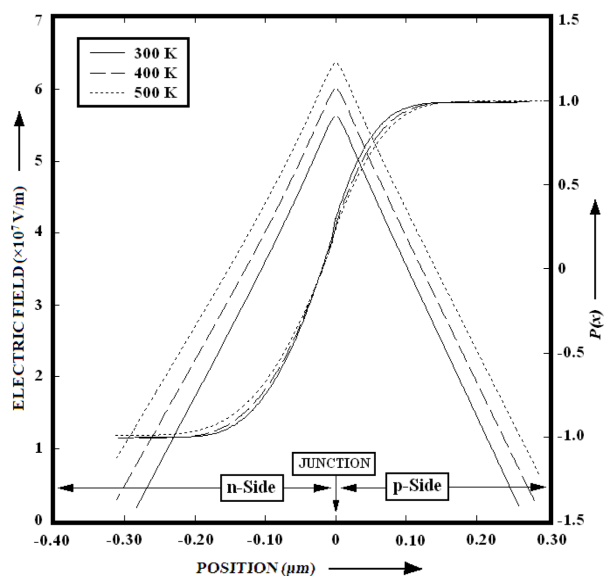

Figure 1: Electric field and normalized current density profiles of W-band DDR Silicon IMPATT device at different junction temperatures ($J_0 = 3.2\times10^8$ Amp/m^2).

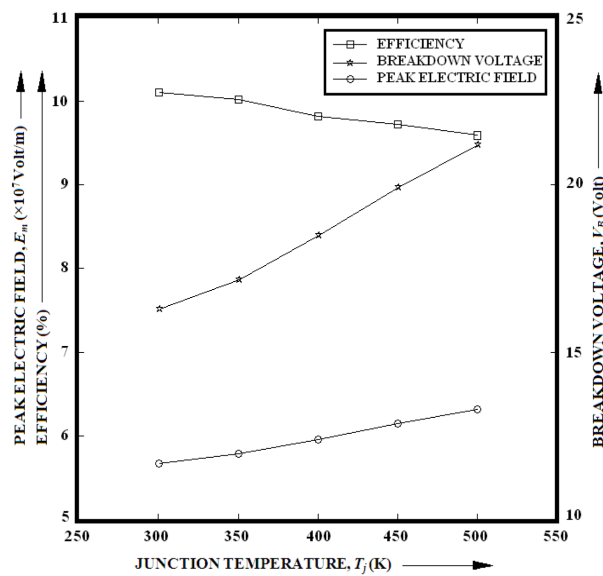

Figure 2: Variation of peak electric field, breakdown voltage and efficiency of W-band DDR Silicon IMPATT device with junction temperature ($J_0 = 3.2\times10^8$ Amp/m^2).

Figure 3 shows the admittance characteristics of the device at the optimum bias current density of, $J_0 = 3.2\times10^8$ Amp/m^2 for different junction temperatures. The magnitude of negative conductance of the device decreases with increasing junction temperature. The distribution of negative resistivity within the depletion layer of the device i.e. the negative resistivity profile of the device at different junction temperatures are shown in Figure 4. The variations of negative conductance, negative resistance and Q-factor of W-band DDR Silicon IMPATT device at optimum bias current density with junction temperature are shown in Figure 5. Figure 6 shows the variation of peak optimum frequency and RF power output at optimum bias current density of W-band DDR Silicon IMPATT device with junction temperature. It is interesting to observe that the device oscillates at higher frequencies at lower junction temperatures. It can be also noted from Figure 6 that the device delivers higher output power at higher junction temperatures. The peak operating frequency of the device decreases by *31%*, while the RF power output increases

by *23%* when the junction temperature rises from *300 K* to *500 K*. The simulated value of RF power output is found to be in very close agreement with experimental value reported in [15] at realistic junction temperature of *500 K*.

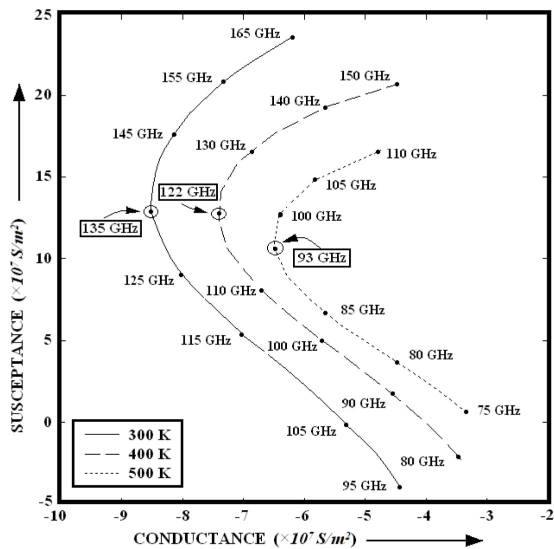

Figure 3: Admittance characteristics of W-band DDR Silicon IMPATT device at different junction temperatures ($J_0 = 3.2\times10^8$ Amp/m^2).

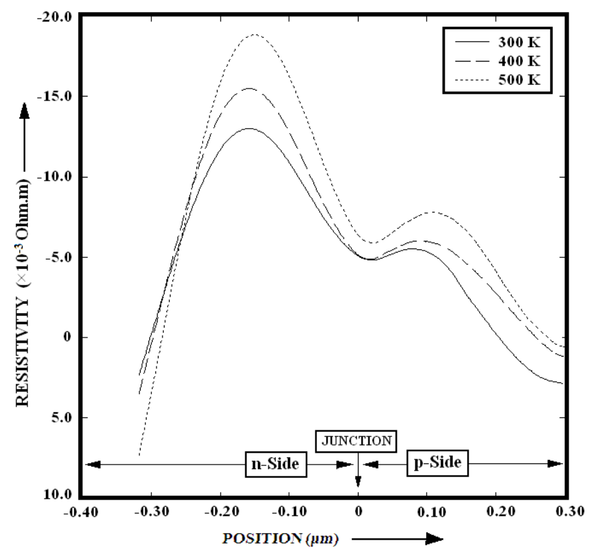

Figure 4: Negative resistivity profiles of W-band DDR Silicon IMPATT device at different junction temperatures ($J_0 = 3.2\times10^8$ Amp/m^2).

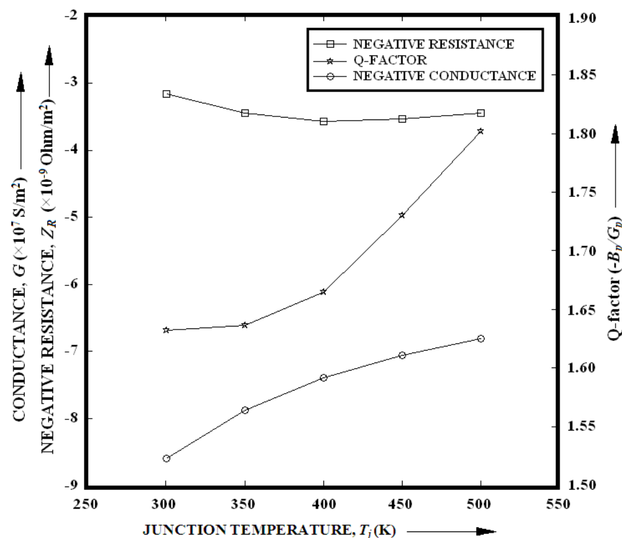

Figure 5: Variation of negative conductance, negative resistance and Q-factor of the W-band DDR Silicon IMPATT device with junction temperature ($J_0 = 3.2\times10^8$ Amp/m^2).

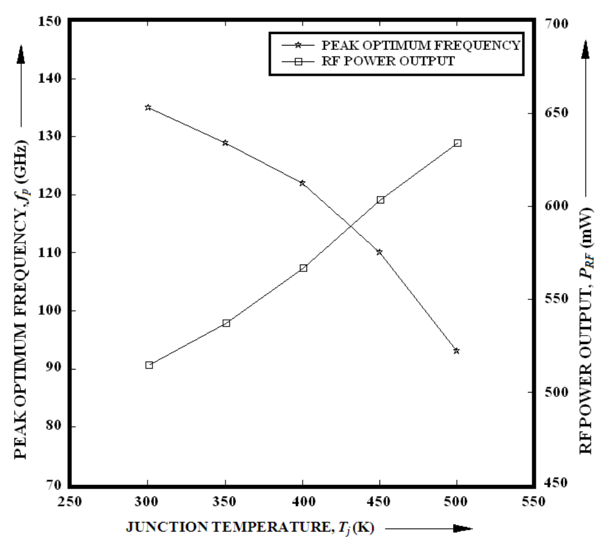

Figure 6: Variation of peak optimum frequency and RF power output of the W-band DDR Silicon IMPATT device with junction temperature ($J_0 = 3.2\times10^8$ Amp/m^2).

V. CONCLUSION

The effect of junction temperature of the DC and high-frequency properties of W-band DDR Silicon IMPATT device is investigated in this paper. It is observed that the DC and small-signal properties of the device depend strongly on the junction temperature. The RF power output of the device is higher at higher junction temperature. But the junction temperature of the device should not be allowed to rise above *575 K* which is the burn out

temperature of the Silicon based IMPATTs. In practical cases, the device junction temperature is kept fixed at about *500 K* during the steady state CW operation of IMPATT oscillator by using proper heat sink arrangement.

References

[1] T. A. Midford and R. L. Bernick, "Millimeter -wave CW IMPATT diodes and Oscillators", IEEE Trans. Microwave Theory Tech., **27**, 483 (1979).

[2] Y. Chang, J. M. Hellum, J. A. Paul and K. P. Weller, "Millimeter-wave IMPATT Sources for Communication Applications", IEEE MTT-S International Microwave Symposium Digest, 216-219 (1977).

[3] W. W. Gray, L. Kikushima, N. P. Morentc and R. J. Wagner, "Applying IMPATT Power Sources to Modern Microwave Systems". IEEE Journal of Solid-State Circuits, **4**, 409-413 (1969).

[4] D. Ghoshal, "Measurement of electrical resistance of Silicon Single Drift Region IMPATT diode based on the study of the device and mounting circuit at threshold condition", Journal of Electron Devices, **11**, 625-631 (2011).

[5] A. Acharyya and J. P. Banerjee, "Heat Sink Design and Temperature Distribution Analysis for Millimeter Wave IMPATT Oscillators using Finite Difference Method", Archives of Applied Science Research, **3**, 107-120 (2011).

[6] A. Acharyya, J. Mukherjee, M. Mukherjee and J. P. Banerjee, "Heat Sink Design for IMPATT Diode Sources with Different Base Materials Operating at 94 GH*z*", Archives of Physics Research, **2**, 107-126 (2011).

[7] A. Acharyya and J. P. Banerjee, "Heat Sink Temperature Profile of Ring Geometry DDR IMPATT Diode", Journal of Telecommunications, **6**, 27-31 (2010).

[8] A Acharyya, B. Pal and J. P. Banerjee, "Temperature Distribution inside Semi-Infinite Heat Sinks for IMPATT Sources", International Journal of Engineering Science and Technology, **2**, 5142-5149 (2010).

[9] A. Acharyya, B. Pal and J. P. Banerjee, "Comparison Between 2-D Temperature Distribution Analysis Inside a Semi-infinite Copper Heat Sink for Mesa and Ring Structure of Si-IMPATT Diodes using Analytical Method and Finite Difference Method", International Journal of Electronic Engineering Research, **2**, 553-567 (2010).

[10] "Electronic Archive: New Semiconductor Materials, Characteristics and Properties," http://www.ioffe.ru/SVA/NSM/Semicond.

[11] S. M. Sze, and R. M. Ryder, "Microwave Avalanche Diodes", Proc. of IEEE, Special Issue on Microwave Semiconductor Devices, **59**, 1140-1154 (1971).

[12] S. K. Roy, M. Sridharan, R. Ghosh, and B. B. Pal, "Computer method for the dc field and carrier current profiles in the IMPATT device starting from the field extremum in the depletion layer" Proceedings of the 1st Conference on Numerical Analysis of Semiconductor Devices (NASECODE I), J. H. Miller, Ed., Dublin, Ireland, 266-274 (1979).

[13] S. K. Roy, J.P. Banerjee and S. P. Pati, "A Computer analysis of the distribution of high frequency negative resistance in the depletion layer of IMPATT Diodes" Proc. 4th Conf. on Num. Anal. of Semiconductor Devices (NASECODE IV) (Dublin) (Dublin: Boole), 494-500 (1985).

[14] H. K. Gummel and J. L. Blue, "A small-signal theory of avalanche noise in IMPATT diodes", IEEE Trans. on Electron Devices, **14**, 569-580 (1967).

[15] J. F. Luy, A. Casel, W. Behr and E. Kasper, 'A 90-GHz double-drift IMPATT diode made with Si MBE', IEEE Trans. Electron Devices, **34**, 1084-1089 (1987).

[16] W. N. Grant, "Electron and hole ionization rates in epitaxial Silicon", Solid State Electron, **16**, 1189-1203, (1973).

[17] C. Canali, G. Ottaviani and A. A. Quaranta, "Drift velocity of electrons and holes and associated anisotropic effects in silicon", J. Phys. Chem. Solids, **32**, 1707 (1971).

[18] B. Van Zeghbroeck, "Principles of Semiconductor Devices" (2011).