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CALCULATION OF AVALANCHE RESPONSE TIME FOR DETERMINING THE HIGH FREQUENCY PERFORMANCE LIMITATIONS OF IMPATT DEVICES

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ABSTRACT
The high frequency performance limitations of Si, GaAs and InP IMPATT devices based on avalanche response time is investigated in this paper. Drift-diffusion model is used to design SDR IMPATTs based on Si, GaAs and InP at different millimeter-wave and sub-millimeter-wave frequencies and corresponding avalanche response times and associated avalanche delay as well as transit times are calculated. Results show that the high frequency limits of GaAs and Si IMPATT devices are 147 GHz and 500 GHz respectively. It is observed that InP IMPATTs are highly suitable for operation at higher mm-wave and terahertz frequencies due to smaller value of avalanche response time of InP as compared to Si and GaAs.

Keywords: Avalanche Response Time, Transit Time, SDR IMPATTs, High Frequency Limitation.

I. INTRODUCTION

Impact Avalanche Transit Time (IMPATT) diodes have emerged as powerful solid state sources capable of delivering sufficient power at microwave, millimeter-wave and sub-millimeter-wave regions [1]. During the initial phases of development of IMPATT devices in late sixties and early seventies, germanium and silicon were mainly used as semiconducting materials for IMPATT fabrication. Due to very low power capability, Ge IMPATTs have now become obsolete. In the seventies the rapid development of silicon technology has made possible the practical realization of Si single drift and double drift IMPATTs which can provide RF power of the order of several watts at microwave and mm-wave bands. It may be noted that the DC to RF conversion efficiency and RF power output of Si IMPATTs fall sharply at higher mm-wave frequencies. GaAs also emerged as a highly suitable material for IMPATT action in the lower microwave frequency range (*8-40 GHz*). Significant improvement in the microwave performance of GaAs IMPATTs over Si IMPATTs has been achieved at lower microwave frequencies ranging between C and X-band up to *40 GHz*. Chang et al reported that GaAs IMPATTs can deliver few milliwatts of power with low conversion efficiency at *130 GHz* [2]. Experimental work on GaAs IMPATTs by Huang et al shows that both the power output and efficiency of GaAs IMPATTs are quite high in the lower frequency bands which fall sharply at mm-wave frequencies [3]. Another III-V semiconductor material InP IMPATTs are highly suitable for high power, high efficiency mm-wave and sub-mm-wave performance [4-5] Ion-implanted SDR IMPATTs based on InP has been reported by Berenz et al at X-band frequencies providing good microwave performance [6].

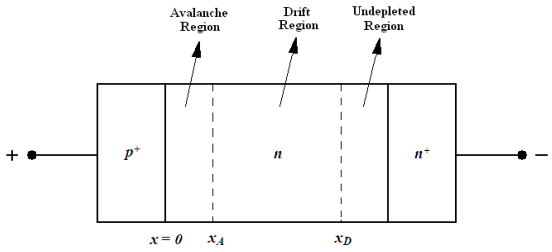

Figure 1: Schematic of a reverse biased flat SDR.

The high frequency performance of IMPATTs depends on material parameters (carrier ionization rates, drift velocities etc) of base semiconductor material [7]. The drift velocities of charge carriers (electrons and holes) in most semiconductors increase linearly with electric field at low-field range due to the acoustic phonon scattering. However, at higher fields ($\xi > 10^6$ *V/m*) the dominant scattering is due to optical phonons arising from high thermal vibrations of the lattice as a result of which the drift velocity of charge carriers saturates. Thus the transit time ($(x_D - x_A)/v_s$) required by the charge carriers to cross the depletion region of IMPATT device is proportional to the depletion layer width (x_D), since the drift velocity (v_s) is constant at higher field range. The avalanche response time of the charge carriers (electrons and holes) is related to the avalanche multiplication process and plays an important role in determining the high frequency performance of the device. One dimensional reverse biased flat profile p^+nn^+ single drift region (SDR) IMPATT structure shown in Figure 1 is considered in our analysis to determine the avalanche response time. If τ_{an} and τ_{ap} be the avalanche response times initiated by electrons and holes respectively, then these are expressed as [8],

$$\tau_{an} = \frac{1}{(v_{sn} + v_{sp})} \int_0^{x_A} exp\left[-\int_0^x (\alpha - \beta) dx' \right] dx \qquad (1)$$

$$\tau_{ap} = \tau_{an} \exp\left[\int_0^{x_A} (\alpha - \beta) dx\right] \quad (2)$$

When avalanche process is initiated by a mixture of electrons and holes then the corresponding response time τ_a is given by [8],

$$\tau_a = \tau_{an}\left\{(1-k) + k.\exp\left[-\int_0^{x_A} (\alpha - \beta) dx\right]\right\}^{-1} \quad (3)$$

Where α and β are the ionization rates of electrons and holes respectively and $k = J_{ps}/J_s$ and $(1\text{-}k) = J_{ns}/J_s$; where $J_s = J_{ps} + J_{ns}$ is the reverse saturation current of the device. Avalanche response time leads to the avalanche phase delay in IMPATT device. The avalanche phase delay can be determined from the location of negative resistivity profile ($R(x)$) peak from the junction of the device. If the distance of the $R(x)$-peak from the junction is x_p and corresponding optimum frequency is f_{opt}, then the avalanche phase delay at x_p can be obtained from the following relation [9],

$$\varphi_A = \frac{2\pi x_p f_{opt}}{v_{sn}} \quad (4)$$

Where, v_{sn} is the saturated drift velocity of electrons in a p^+nn^+ SDR IMPATT.

II. DESIGN AND SIMULATION

The frequency of operation of an IMPATT diode essentially depends on the transit time of charge carriers to cross the depletion layer of the diode. IMPATT devices based on GaAs, Si and InP having single drift p^+nn^+ structure are first designed for operation at different mm-wave and sub-mm-wave frequencies by using computer simulation technique and the transit time formula proposed by Sze and Ryder [10] given by $x_D = 0.37\ v_{sn} / f_d$; where x_D, v_{sn} and f_d are the total depletion layer width, saturated drift velocity of electrons and design frequency respectively. The doping concentrations of n^+ & p^+-highly doped substrates are taken to be $N_{sub} = 10^{26}\ m^{-3}$. The background doping concentrations of n and p-depletion regions are initially chosen according to the design frequency. The electric field profile using the above doping profile is obtained from the computer simulation [11]. The input doping profile is adjusted so that the electric field just punches through the depletion layer (x_D) for a particular value of f_d and a particular biasing current density J_0. A double iterative small-signal computer simulation [12-15] based on Gummel-Blue approach [16] is then carried out to obtain the admittance characteristics of the device. The optimum frequency (f_{opt}) for peak negative conductance is determined from the admittance characteristics. If the magnitude of f_{opt} differs very much from f_d, the value of J_0 is varied and the computer simulation program is run till the value of f_{opt} is nearly equal to the value of f_d. The bias current density (J_0) is thus fixed for the particular design frequency.

The design parameters of IMPATT devices based on GaAs, Si and InP based SDR IMPATTs are listed in Table I. The admittance characteristics of GaAs, Si and InP IMPATTs at different mm-wave and sub-mm-wave frequency bands are shown in Figure 2, 3 and 4 respectively. The recently reported experimental values of material parameters at *500 K* temperature are used in our simulation [7].

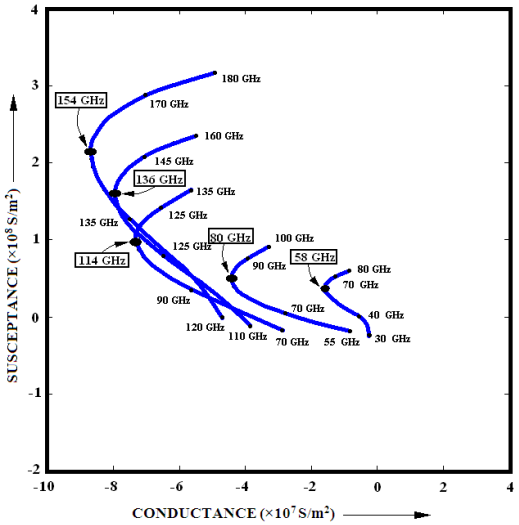

Figure 2: Small-signal admittance characteristics of GaAs based SDR IMPATTs.

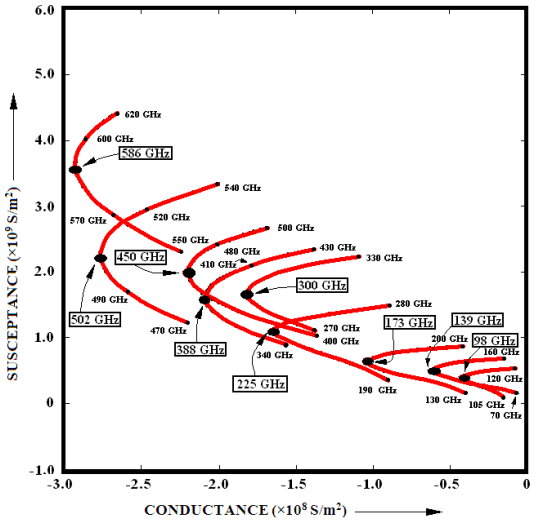

Figure 3: Small-signal admittance characteristics of Si based SDR IMPATTs.

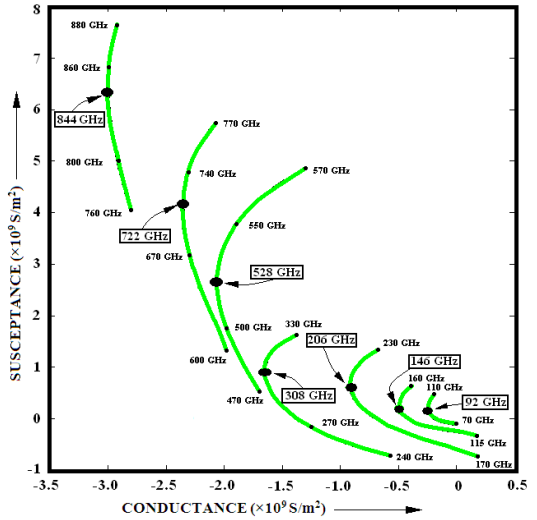

Figure 4: Small-signal admittance characteristics of InP based SDR IMPATTs.

TABLE I. Design Parameters

BASE MATERIAL	DESIGN FREQUENCY, f_d (GHz)	n-EPITAXIAL LAYER THICKNESS, x_D (μm)	n-EPITAXIAL LAYER DOPING, N_D ($\times 10^{23}\ m^{-3}$)	SUBSTRATE LAYER DOPING, N_{Sub} ($\times 10^{26}\ m^{-3}$)	BIAS CURRENT DENSITY, J_0 ($\times 10^{8}\ Amp/m^2$)
GaAs	58	0.4800	0.600	1.0	1.5
	80	0.4000	1.200	1.0	5.0
	114	0.3000	1.800	1.0	10.0
	136	0.2500	1.950	1.0	12.0
	154	0.2200	2.100	1.0	14.0
Si	98	0.3200	1.450	1.0	5.0
	139	0.2800	1.800	1.0	6.5
	173	0.2400	2.200	1.0	12.0
	225	0.1750	3.950	1.0	15.0
	300	0.1400	5.200	1.0	18.0
	388	0.1200	6.500	1.0	22.0
	450	0.1100	7.500	1.0	25.0
	502	0.0900	8.500	1.0	30.5
	606	0.0800	9.300	1.0	36.0
InP	92	0.3500	1.600	1.0	1.4
	146	0.2500	2.200	1.0	4.0
	206	0.1800	3.500	1.0	7.0
	308	0.1200	6.100	1.0	10.0
	528	0.0700	10.50	1.0	18.0
	722	0.0600	11.50	1.0	20.0
	844	0.0500	14.50	1.0	22.0

III. RESULTS AND DISCUSSION

III.1 DC Results

Simulation of the DC properties of designed devices is carried out by using the double iterative field maximum technique to obtain the electric field profiles and current density profiles [11]. DC program also provides breakdown voltage and DC to RF conversion efficiency of the device. Variations of breakdown voltage, peak electric field and efficiency of GaAs, Si and InP SDRs with frequency are shown in Figure 5.

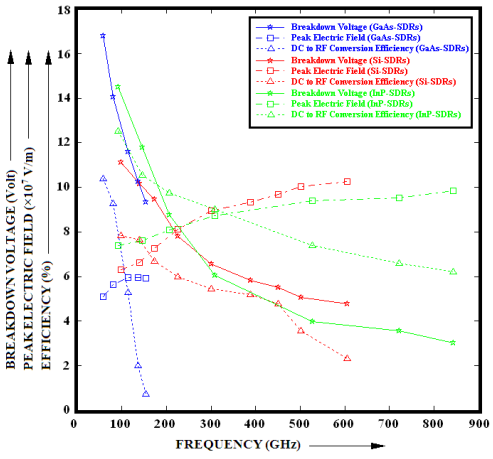

Figure 5: Variations of Breakdown Voltage, Peak Electric Field and DC to RF Conversion Efficiency of GaAs, Si and InP based SDR IMPATTs with Frequency.

Figure 5 shows that peak electric field of the devices increase with frequency but the breakdown voltage and DC to RF conversion efficiency of the devices decrease with frequency. It is interesting to observe that the efficiency of GaAs SDR IMPATTs decreases sharply with frequency and reduces to *0.72%* at *154 GHz*. It is also interesting to note that the efficiencies of InP SDR IMPATTs are sufficiently higher at higher frequencies (*13.20%* at *844 GHz*) as compared to corresponding Si SDR IMPATTs for which the efficiency falls to *2.30%* at *606 GHz*.

III.2 Avalanche Response Time Calculation

Equations (1) and (3) are incorporated in the DC program to determine the avalanche response time of p^+nn^+ SDR IMPATTs based on GaAs, Si and InP at different mm-wave and sub-mm-wave frequencies. Variations of avalanche response time and transit time of the devices with frequency are shown in Figure 6.

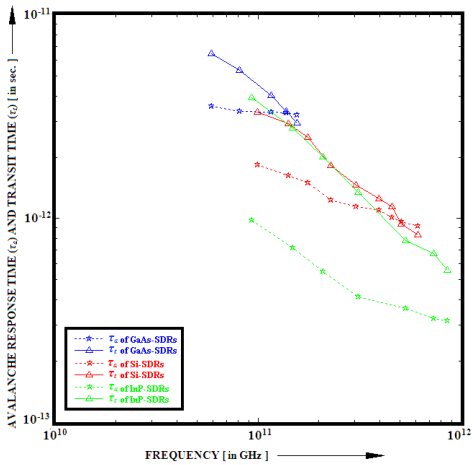

Figure 6: Variations of Avalanche Response Time and Transit Time with frequency.

Figure 6 shows that the avalanche response times of InP SDRs are much smaller than those of GaAs and Si SDRs. It is also noted that the avalanche response time of GaAs and Si devices exceeds the transit time of those devices at *147 GHz* and *500 GHz* approximately. So

above those frequencies, the IMPATT action will not produce high frequency power in GaAs and Si IMPATTs. The above mentioned frequencies are therefore the upper frequency limits of GaAs and Si IMPATTs. In case of InP IMPATTs, the avalanche response time remains well below the transit time of the device even at *844 GHz*. So it can be concluded that InP IMPATTs are more suitable at higher sub-mm-wave (terahertz regime) frequencies as compared to GaAs and Si counterparts.

III.3 Avalanche Phase Delay Calculation

A computer simulation method [12-15] is used to obtain the negative resistivity (*R(x)*) profiles of SDR GaAs, Si and InP IMPATTs at different frequencies. The results are shown in Figure 7.

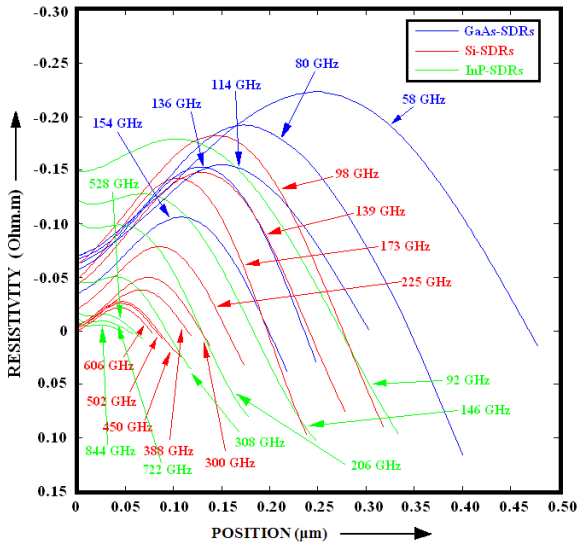

Figure 7: Negative Resistivity Profiles of GaAs, Si, InP based SDR IMPATTs.

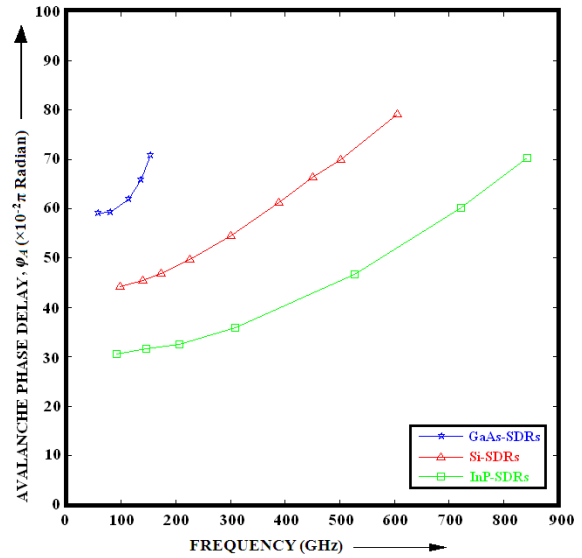

Figure 8: Variations of Avalanche Phase Delay in GaAs, Si, InP based SDR IMPATTs with frequency.

Using equation (4) the avalanche phase delays of IMPATTs based on different materials at different frequencies are calculated from the *R(x)*-profiles shown in Figure 8. It is observed that the avalanche phase delay of the devices increases with frequency. Terminal current must be 180^0 out of phase with the RF voltage in IMPATT device to obtain the maximum negative resistance. Avalanche phase delay and Transit time delay together constitute the total avalanche transit time (ATT) phase delay of 180^0 between terminal current and RF voltage to get the maximum RF power output. Any phase-difference other than 180^0 but lying in between 90^0 and 270^0 causes lower RF power output. For GaAs and Si IMPATTs avalanche phase delays are higher which leads to total ATT phase difference values higher than 180^0. Thus the efficiency as well as RF power output of the devices decreases rapidly at higher frequencies. But in InP IMPATTs avalanche phase delay is lower than those in GaAs and Si IMPATTs. This explains why DC to RF conversion efficiency and power output is higher for InP IMPATTs at higher sub-mm-frequencies.

IV. CONCLUSIONS

In this paper the high frequency performance limitations of Si, GaAs and InP IMPATT devices based on avalanche response time is studied. Results show that the high frequency limits of GaAs and Si based IMPATT devices are *147 GHz* and *500 GHz* respectively. Above these frequencies IMPATT operation is not possible for GaAs and Si devices. But InP IMPATTs are highly suitable at higher mm-wave upto terahertz frequency of operation due to their lower value of avalanche response time.

References

[1] T. A. Midford and R. L. Bernick, "Millimeter Wave CW IMPATT diodes and Oscillators", IEEE Trans. Microwave Theory Tech., **27**, 483 (1979).

[2] K. Chang, J. K. Kung, P. G. Asher, G. M. Hayshibara and R. S. Ying, "GaAs Read type Impatt diode for 130 GHz CW operation", Electronics Letters, **17**, 471 (1981).

[3] H. C. Huang, P. A. Levine, A.R. Gobat and J. B. Klatskin, "High frequency operation of GaAs Schottky barrier Impatts", Proc. IEEE, **60**, 464 (1972).

[4] S. K. Roy and J. P. Banerjee, "properties of gallium arsenide and indium Phosphide impatts at microwave and millimeter-wave frequencies", Bull. Mater. Sci., **13 (1&2)**, 113 (1990).

[5] R. Mukherjee and J. P. Banerjee, "Avalanche and drift layer contribution to the negative resistance

of millimeter wave p^+nn^+ InP IMPATT diode for different current densities", Int. J. Electronics, **76**, 589 (1994).

[6] J. J. Berenz, F. B. Frank and T. L. Hierl, "Ion implanted p-n junction indium Phosphide IMPATT diodes", Electronics Letters, **14**, 683 (1978).

[7] "Electronic Archive: New Semiconductor Materials, Characteristics and Properties," http://www.ioffe.ru/SVA/NSM/Semicond.

[8] H. P. Vyas, PhD Dissertation.

[9] J. P. Banerjee, R. Mukherjee, J. Mukhopadhyay and P. N. Mallik, "Studies on Avalanche Phase Delay and the Admittance of an Optically Illuminated Indium Phosphide Avalanche Transit Time Diode at Millimeter Wave Window Frequencies", Phys. Stat. Sol. (a), **153**, 567 (1996).

[10] S. M. Sze, and R. M. Ryder, "Microwave Avalanche Diodes", Proc. of IEEE, Special Issue on Microwave Semiconductor Devices, **59**, 1140 (1971).

[11] S. K. Roy, M. Sridharan, R. Ghosh, and B. B. Pal, "Computer methods for the dc field and carrier current profiles in impatt devices starting from the field extremum in the depletion layer", Proc. of NASECODE-I Conf. on Numerical Analysis of Semiconductor Devices (Dublin: Boole Press), pp 266 (1979).

[12] S. K. Roy, J. P. Banerjee and S. P. Pati, "A computer analysis of the distribution of high frequency negative resistance in the depletion layers of impatt diodes", Proc. of NASECODE-IV Conf. on Numerical Analysis of Semiconductor Devices (Dublin: Boole Press), 494 (1985).

[13] A. Acharyya, S. Banerjee and J. P. Banerjee, "Dependence of DC and Small-signal Properties of Double Drift Region Silicon IMPATT Device on Junction Temperature", Journal of Electron Devices, **12**, 725 (2012).

[14] A. Acharyya and J. P. Banerjee, "A Comparative Study on the Effect of Optical Illumination on $Si_{1-x}Ge_x$ and Si Based DDR IMPATT Diodes at W-Band", Iranian Journal of Electronics & Electrical Engineering, **7**, 179 (2011).

[15] A. Acharyya, M. Mukherjee and J. P. Banerjee, "Influence of Tunnel Current on DC and Dynamic Properties of Silicon Based Terahertz IMPATT Source", Terahertz Science and Technology, **4**, 26 (2011).

[16] H. K. Gummel and J. L. Blue, "A Small-Signal Theory of Avalanche Noise in IMPATT Diodes", IEEE Trans. Electron Devices, **14**, 569 (1967).