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MODELING OF 3-D POTENTIAL DISTRIBUTION FOR A THIN FILM FULLY-DEPLETED P-CHANNEL G^4-FET

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Abstract—A mathematical model of potential distribution has been derived and analyzed considering three dimensions of a fully-depleted p-channel G^4-FET. Potential variation between the MOS gates is assumed to be parabolic for thin film devices. Again, potential variation between the drain and source shows parabolic nature due to the presence of MOS gates. Using these two assumptions and with appropriate boundary conditions, the mathematical model is developed by solving Poisson's equation. Using this model, surface potential is studied by changing various parameters and gate voltages. The potential variation between the MOS gates is also studied for different parameters. This model successfully takes into account the effect of all four gates of the transistor and the short channel effect.

Keywords: potential distribution; three-dimensional modeling; short channel effect; surface potential; cross-sectional aspect ratio

I. INTRODUCTION

The international roadmap for semiconductors forecasts a transition from bulk to SOI then from single to multiple gates SOI for high performance digital integrated circuit [1]-[2]. G^4-FET, since its invention from 2002, has been considered as a cardinal solution for this goal [3]. It consists of the maximum number of gates that can be achieved in a single transistor which can be independently biased to modulate the current in the channel. This exciting feature offers functional flexibility for the circuit designers while reducing the number of transistors as compared to the standard CMOS technology [4]. Single transistor logic functions, novel analog signal circuits, low-power modulation for RF applications, and emulation of quantum wires are just a small number of the exciting opportunities envisioned using the G^4-FET and leveraging its multiple gates [5].

A general expression of potential distribution of the fully-depleted device is certainly useful for modeling static parameters and current-voltage characteristics. In an earlier work, an analytical expression of 3-D potential distribution for a fully-depleted n-channel G^4-FET has been derived [4]. In this work, an expression of surface potential distribution for a fully-depleted p-channel G^4-FET has been derived using different assumptions and derivation method. Using this expression a general expression for 3-D potential distribution has been derived.

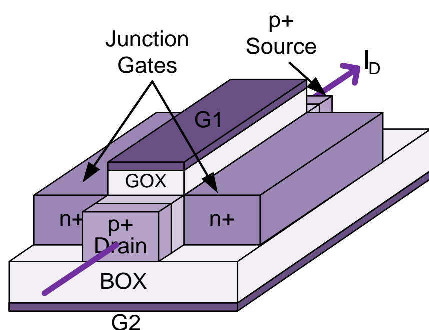

Figure1. p-channel G^4-FET.

In Section II, the G^4-FET structure and operation are explained. The 3-D potential distribution is modeled and verified in Section III. In Section IV, the effect of dimensional parameters on front surface potential is analyzed. In Section V, the same effect is analyzed for potential variation between the MOS gates.

II. DEVICE STRUCTURE

G^4-FET is formed using the normal layout of a SOI MOSFET with two explicit body contacts on opposite sides of MOSFET which are used as source and drain for G^4-FET [6]. The p-channel G^4-FET is actually an n-channel SOI MOSFET. Source and drain of the MOSFET are used as junction-gates for the G^4-FET as shown in Fig. 1. Drain current comprises of the majority carriers which flows in the direction perpendicular to that of a MOSFET [7].

The device considered here is a p-channel fully-depleted thin film G^4-FET, where the maximum depletion depth is greater than the silicon film thickness [8]. When the device is turned off, the silicon film is fully-depleted due to the presence of positive interface charges and to the negative value of the work function difference between the n+ poly-silicon gate to the p-type body of the device [9].

III. MODEL DERIVATION AND VERIFICATION

The source of the considered G^4-FET is kept grounded and the drain is kept at a voltage (V_D). Front-gate voltage (V_{G1}), back-gate voltage (V_{G2}) and junction-gate voltages ($V_{JG1,2}$) are such that the channel is fully-depleted.

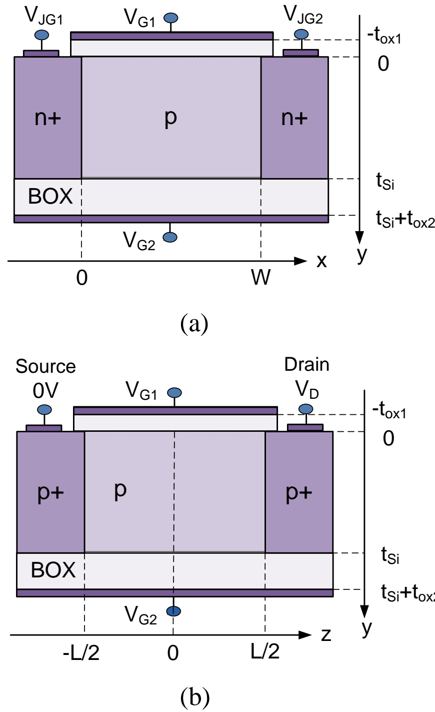

Figure 2. Cross-sections of a p-channel G[4]-FET showing axes and necessary symbols for modeling. The drain current direction is (a) perpendicular to the figure. (b) from right to left of the figure.

Along the channel, potential gradually changes from zero at source to V_D at drain. In this work, it is assumed that this variation is parabolic due to MOS gates. This assumption was previously used for 3-D modeling of an n-channel G[4]-FET [5]. The body potential can be expressed with respect to the source (which is kept at ground potential) as

$$\Psi(x,y,z) = a(x,y)z^2 + b(x,y)z + c(x,y) \tag{1}$$

The boundary conditions along   -direction are given by

$$\psi(x,y,-\tfrac{L}{2}) = 0 \tag{2a}$$

$$\psi(x,y,\tfrac{L}{2}) = V_D \tag{2b}$$

where, L is the channel length. Using these boundary conditions, the coefficients of (1) can be obtained as

$$c(x,y) = \psi(x,y,0) \tag{3a}$$

$$b(x,y) = \frac{V_D}{L} \tag{3b}$$

$$a(x,y) = \frac{2V_D - 4\psi(x,y,0)}{L^2} \tag{3c}$$

Substituting the coefficients into (1) yields

$$\Psi(x,y,z) = \Psi(x,y,0)\left(1 - \frac{4z^2}{L^2}\right) + \left(\frac{2V_D}{L^2}\right)z^2 + \left(\frac{V_D}{L}\right)z \tag{4}$$

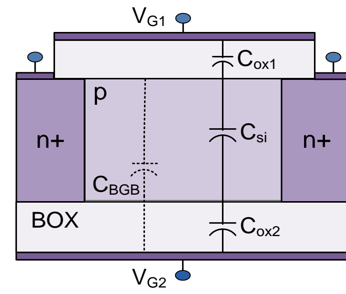

Figure 3. Cross-section of p-channel G[4]-FET showing different capacitances used in the derivation.

Using full-depletion approximation 3-D Poisson's equation

$$\frac{\partial^2 \Psi(x,y,0)}{\partial x^2} + \frac{\partial^2 \Psi(x,y,0)}{\partial y^2} + \frac{\partial^2 \Psi(x,y,0)}{\partial z^2} = \frac{qN_A}{\epsilon_{Si}} \tag{5}$$

Substituting (4) into (5) and then reducing it to z=0 plane yields

$$\frac{\partial^2 \Psi(x,y,0)}{\partial x^2} + \frac{\partial^2 \Psi(x,y,0)}{\partial y^2} - \left(\frac{8}{L^2}\right)\Psi(x,y,0) + \left(\frac{4}{L^2}\right)V_D = \frac{qN_A}{\epsilon_{Si}} \tag{6}$$

where, N_A is the doping concentration of channel and ϵ_{Si} is the permittivity of silicon. The dependence of $\psi(x,y,0)$ can be approximated by a simple parabolic function as [10]

$$c(x,y) = \psi(x,y,0) = f(x)\,y^2 + g(x)y + h(x) \tag{7}$$

This type of assumption is very common for modeling of device parameters [3]-[4]. The boundary conditions along direction can be stated as

$$\left.\frac{d\Psi(x,y,0)}{dy}\right|_{y=0} = \left(\frac{\epsilon_{ox}}{\epsilon_{si}}\right)\left(\frac{\Psi_{s1}(x) - V_{G1}}{t_{ox1}}\right) \tag{8a}$$

$$\left.\frac{d\Psi(x,y,0)}{dy}\right|_{y=t_{Si}} = \left(\frac{\epsilon_{ox}}{\epsilon_{si}}\right)\left(\frac{V_{G2} - \Psi_{s2}(x)}{t_{ox2}}\right) \tag{8b}$$

where, $\psi_{s1}(x) = \psi(x,0,0)$ is the front surface potential distribution, $\psi_{s2}(x) = \psi(x,t_{Si},0)$ is the back surface potential and $V'_{G1} = V_{G1,2} - V_{fb1,2}$. Here, t_{Si} is the silicon film thickness, $t_{ox1,2}$ is the front and back oxide thickness, ϵ_{si} is the dielectric constant of silicon, ϵ_{ox} is the dielectric constant of oxide, $V_{fb1,2}$ are the flat-band voltages. Using (8a) and (8b) the coefficients of (7) can be obtained as

$$h(x) = \psi(x,0,0) = \psi_{s1}(x) \tag{9a}$$

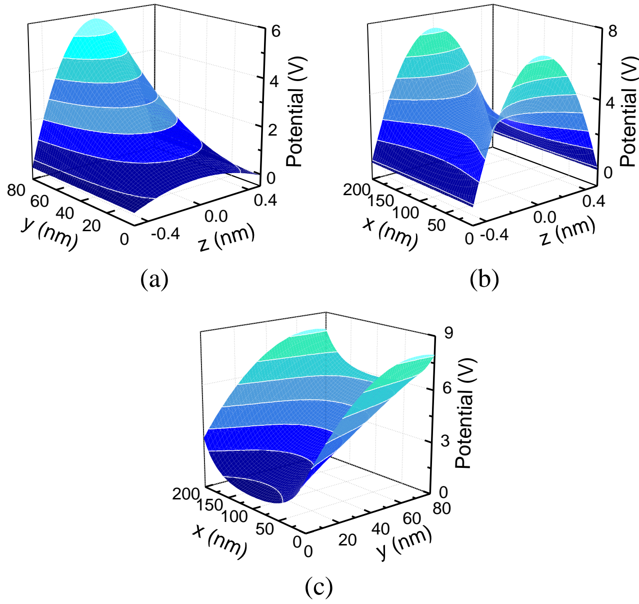

Figure 4. Potential distribution along various planes in the body of a p-channel G[4]-FET. Potential distribution along (a) x=W/2 plane. (b) $y=t_{si}/2$ plane. (c) z=0 plane. Structural parameters: W=200nm, L=1μm, t_{si}=40nm, t_{ox1}=7nm, t_{ox2}=400nm, $N_A=10^{16}cm^{-3}$. Bias conditions: V_{G1}=-0.75V, V_{G2}=60V, V_{JG1}=2V, V_{JG2}=2V and V_D=-50mV.

$$g(x) = \left(\frac{\epsilon_{ox}}{\epsilon_{si}}\right)\left(\frac{\Psi_{s1}(x) - V_{G1}}{t_{ox1}}\right) \quad (9b)$$

$$f(x) = \frac{-\left(1+\frac{C_{ox1}}{C_{BGB}}\right)\Psi_{s1}(x) + \left(\frac{C_{ox1}}{C_{BGB}}\right)V'_{G1} + V'_{G2}}{t_{si}^2\left(1+\frac{2C_{si}}{C_{ox2}}\right)} \quad (9c)$$

where, $C_{BGB} = \left(\frac{1}{C_{si}} + \frac{1}{C_{ox2}}\right)^{-1}$ is defined as back-gate to body capacitance, C_{si} is the silicon film capacitance, $C_{si} = \frac{\epsilon_{si}}{t_{si}}$ is the front-gate oxide capacitance and $C_{ox1} = \frac{\epsilon_{ox}}{t_{ox1}}$ is the back-gate oxide capacitance. These capacitances are shown in Fig. 3. Substituting (9a)-(9c) in (7) and then (7) into (6) yields

$$\frac{d^2\Psi_{s1}(x)}{dx^2} - 2(\alpha+\beta+\frac{4}{L^2})\Psi_{s1}(x) + \left(\alpha V'_{G1} + \beta V'_{G2} + \frac{4}{L^2}V_D\right) = \frac{qN_A}{\epsilon_{si}} \quad (10)$$

where,

$$\alpha = \frac{\frac{C_{ox1}}{C_{BGB}}}{t_{si}^2\left(1+\frac{C_{si}}{C_{ox2}}\right)} \quad (11)$$

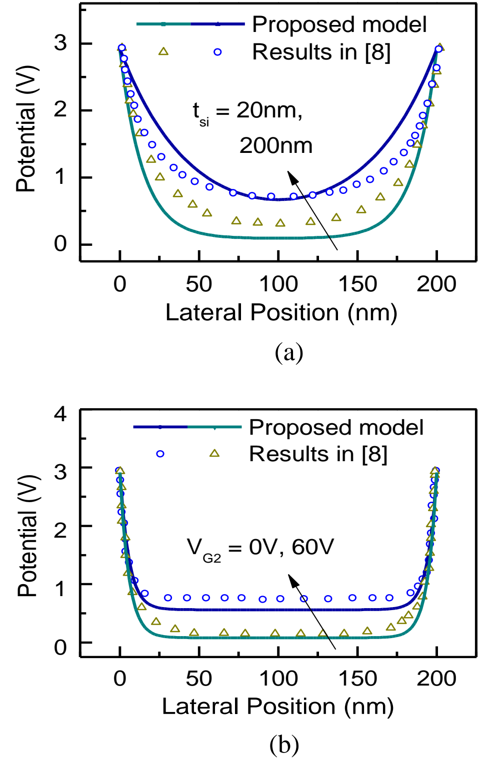

Figure 5. Simulation results for the front surface potential profiles (referenced to source potential) between the junction-gates at mid-length of a 1μm long p-channel G[4]-FET. (a) Narrow channel case (W=200nm) for various silicon film thicknesses and V_{JG}=2V, V_{G2}=0V and V_{G1}=-0.75V. (b) Wide channel case (W=1μm and t_{si}=80nm) for a depleted (V_{G2}=0V) and inverted (V_{G2}=60V) back surface. Structural parameters: t_{ox1}=7nm, t_{ox2}=400nm, $N_A=10^{16}cm^{-3}$.

And
$$\beta = \frac{1}{t_{si}^2\left(1+\frac{C_{si}}{C_{ox2}}\right)} \quad (12)$$

Two more boundary conditions along x-direction are required to solve this differential equation.

$$\psi_{s1}(0) = \phi_b + V_{JG1} \quad (13a)$$

$$\psi_{s1}(W) = \phi_b + V_{JG2} \quad (13b)$$

Where, ϕ_b is the potential barrier between body and junction-gates. The solution of (10) gives the general expression of front surface potential at z=0 plane which is given by

$$\Psi_{s1}(x) = \sigma_s + \frac{(\Phi_b + V_{JG2} - \sigma_s)\sinh(\gamma x) - (\Phi_b + V_{JG1} - \sigma_s)\sinh\{\gamma(x-W)\}}{\sinh(\gamma W)} \quad (14)$$

Where, $\sigma_s = \frac{1}{\gamma^2}\left(\alpha V'_{G1} + \beta V'_{G2} + \left(\frac{4}{L^2}\right)V_D - \frac{qN_A}{\epsilon_{si}}\right)$ (15)

and $$\gamma = \sqrt{(2\left(\alpha + \beta + \frac{4}{L^2}\right)} \qquad (16)$$

Combining (4), (7) and (14), the overall expression of potential can be found as (17) which is shown in the box.

The simulated results are shown in Fig. 4 for various planes. As observed from Fig. 4(a), the maximum front surface potential is ~0.7 V which ensures that the front surface is depleted. The maximum back surface potential is ~5.9 V which is greater than classical value (Φ_F is Fermi potential), which ensures that the back surface is in inversion. The proposed model is verified with the simulated results in [8] which shows front surface potential profile for a p-channel thin film fully-depleted G^4-FET. The verification is shown in Fig. 5.

In Fig. 5(a), proposed model is simulated for a narrow device (W=200nm) where both front and back surfaces are depleted (V_{G1}= -0.75V, V_{G2}=0V). In Fig. 5(b), the proposed model is simulated for a wider device (W=1μm), where back surface is depleted for V_{G2}=0V and inverted for V_{G2}=60V. Both simulated results matches well with the results in [8].

. The accuracy of the model is less perfect when the back surface is driven into strong inversion or strong accumulation. When the interfaces are in strong inversion or accumulation, surface potential increases beyond classical values by few thermal voltages [11]. But the model proposed here cannot predict this kind of changes.

IV. FRONT SURFACE POTENTIAL VARIATION

Front surface potential between the junction-gates is analyzed using (17) by varying different parameters and gate voltages. For simplicity, symmetrical junction-gate bias is assumed i.e. $V_{JG1}=V_{JG2}=V_{JG}$ At first, potential distribution of a narrow device (W=200nm) is analyzed for various silicon film thickness. Both front and back surfaces are kept depleted (V_{G1}=-0.75V, V_{G2}=0V). The surface potential at the mid-width between the junction-gates gets lowered as the silicon film gets thinner as shown in Fig. 6(a).

The impact of the junction-gates on the body potential distribution is attenuated for increased W as seen from Fig. 6(b). In Fig. 6(b), a wider device (W=1μm and t_{si}=80nm) is considered for analysis. This insensitivity occurs because of the fact that transistor is thin and rather wide. When the back surface is depleted (V_{G2}=0V), surface potential remains unaffected by the junction-gate voltage except in the close vicinity of junction-gates.

When an inversion layer is induced at the back surface (V_{G2}=60V), the surface potential can be modulated by V_{JG} despite the low cross-sectional aspect ratio of the device. The inversion layer covering the whole back surface, which is of same type as the junction-gates acts as a third junction-gate. The biasing of the back inversion layer to V_{JG} modulates the back surface potential [8]. In the fully-depleted device, the front surface potential is interrelated to the back surface potential by coupling [4]. As a result, the front surface potential is also changed, resulting in a remarkable modulation of the front channel parameters (front channel current, front channel threshold voltage etc.) by the junction-gate voltage.

The potential distribution is also affected by the aspect ratio W/L of the device when the back surface is inverted, as seen from Fig. 6(c). This is because the amount of inversion charge at the inversion region of the back surface depends on *W* and L . But for a depleted back surface, the potential profile remains same irrespective of channel length.

The cross-sectional aspect ratio t_{Si}/W determines the sensitivity of potential distribution to the effect of junction-gate voltage [8]. For a wider device, the effect of the junction-gates on the potential distribution gets attenuated and the potential profile between the junction-gates flattens as shown in Fig. 6(d). For a device with smaller width, potential profile gets modulated by the junction-gates easily.

$$\Psi(x,y,z) = \left[\left\{1 - (\alpha+\beta)\, y^2 + \frac{C_{ox1}}{C_{si}\, t_{si}}\, y\right\}\left\{\sigma_s + (\frac{\Phi_b + V_{JG2} - \sigma_s\,)\ \sinh(\gamma x) - (\Phi_b + V_{JG1} - \sigma_s\,)\ \sinh\{\gamma(x - W)\}}{\sinh(\gamma W)}\right\}\right.$$
$$\left. + (\alpha V'_{G1} + \beta V'_{G2})\, y^2 + \frac{C_{ox1}}{C_{si}\, t_{si}}\, V'_{G1}\, y\right]\left(1 - \frac{4z^2}{L^2}\right) + \left(\frac{2V_D}{L^2}\right) z^2 + \frac{V_D}{L} z \qquad (17)$$

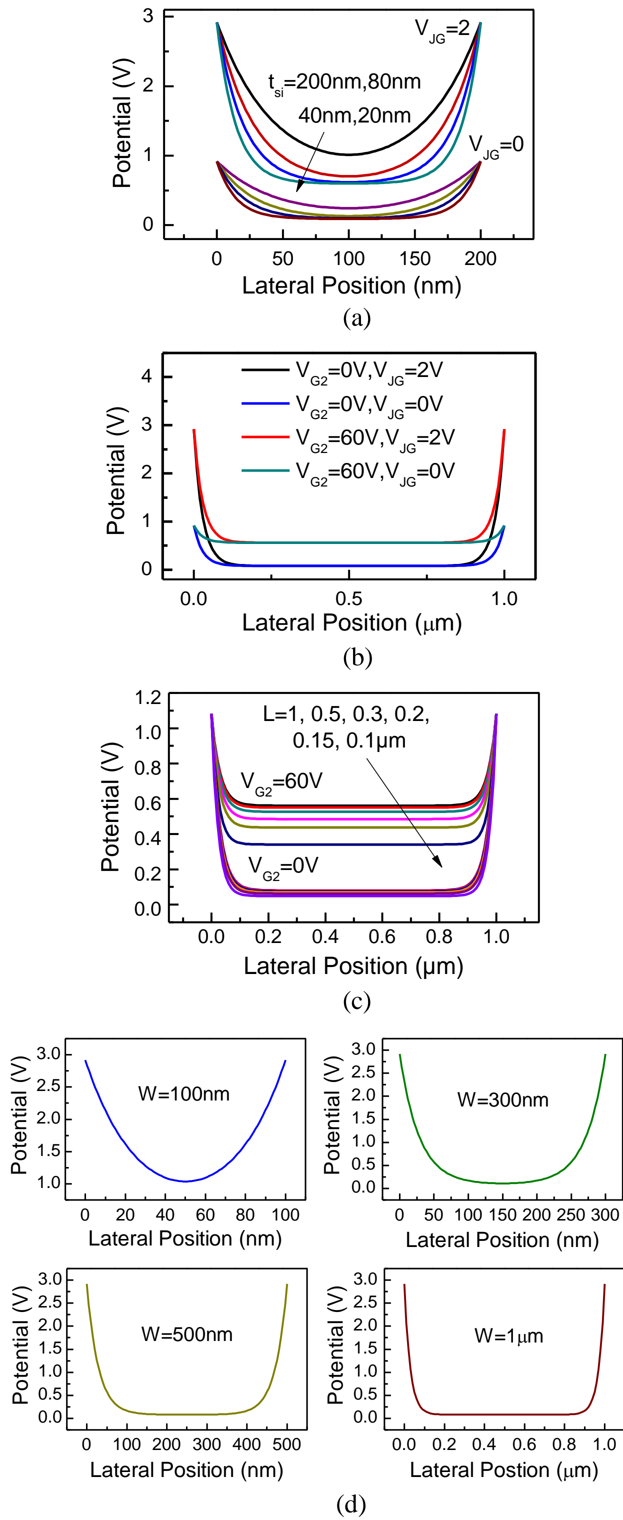

Figure 6. Front surface potential distribution between the junction-gates at mid-length of a p-channel G[4]-FET. (a) Narrow channel case (W=200nm) for various film thicknesses and different V_{JG}. V_{G2}=0V and V_{G1}=-0.75V. (b) Wide channel case (W=1μm and t_{si}=80nm) for a depleted (V_{G2}=0V) and inverted (V_{G2}=60V) back surface for different V_{JG}. (c) Potential distribution for various channel length devices, W=1μm and V_{G1}=-0.75V and V_{JG}=2V (d) Potential distribution for different channel-width (W=100nm, 300nm, 500nm and 1μm) devices. Structural parameters: L=1μm, t_{ox1}=7nm, t_{ox2}=400nm, N_A=10^{16}cm^{-3}.

IV. POTENTIAL VARIATION BETWEEN THE MOS GATES

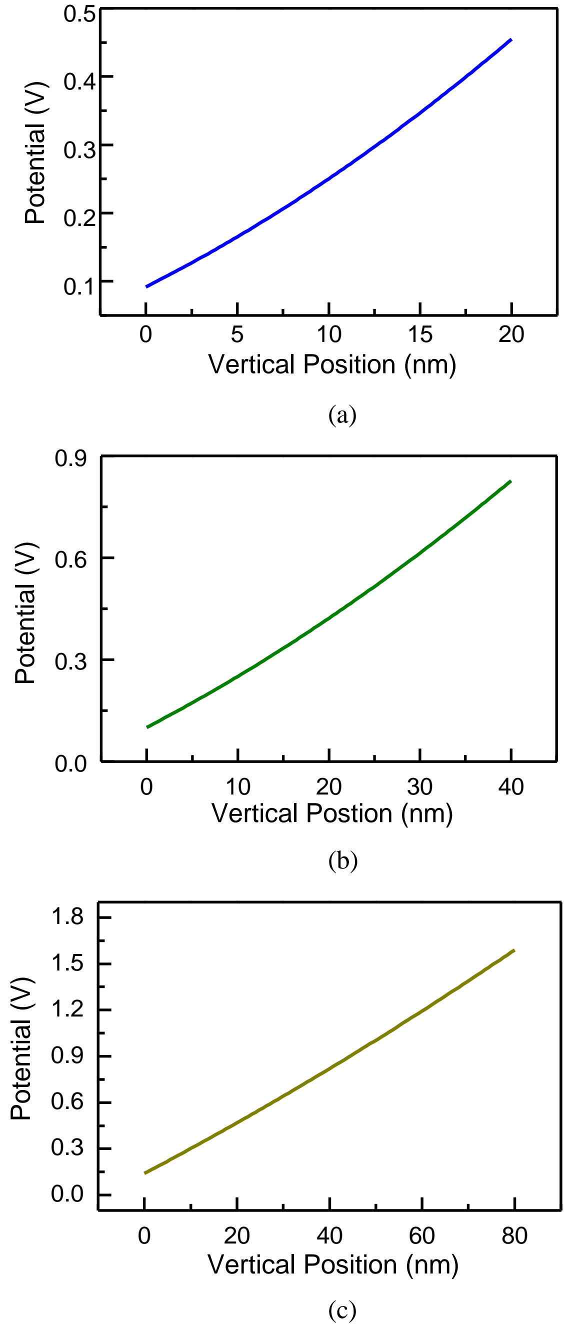

Figure 7. Potential distribution between the MOS gates at mid-length and at mid-width of a narrow p-channel G[4]-FET, keeping both front and back surface depleted. (a) t_{si}=20nm. (b) t_{si}=40nm. (c) t_{si}=80nm. Structural parameters: W=200nm, L=1μm, t_{ox1}=7nm, t_{ox2}=400nm, N_A=10^{16}cm^{-3}.

First, a narrow device (W=200nm) is considered for this analysis and for convenience both front and back surfaces are kept depleted (V_{G1}=-0.75V and V_{G2}=0V). Fig. 7 shows the simulated results of potential distribution between the MOS gates (along -direction) provided by (17) for different silicon film thicknesses. For thinner silicon film devices i.e. for low *cross-sectional* aspect ratio devices, the parabolic nature of the potential profile becomes more visible. For a

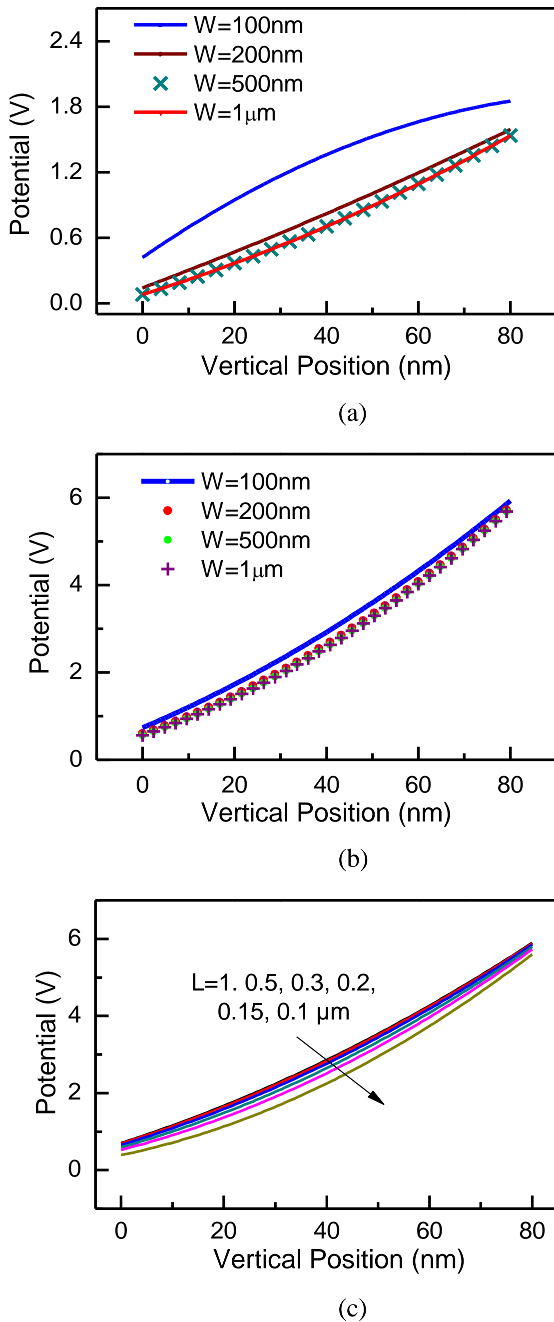

Figure 8. Potential distribution between the MOS gates at mid-length and at mid-width of a p-channel G^4-FET, keeping (a) both front and back surface depleted. (b) front surface depleted and back surface inverted. (c) front surface depleted and back surface inverted and W=200nm. Bias Condition: V_{JG}=2V, V_D=-50mV. Structural parameters: L=1μm, t_{si}=80nm, t_{ox1}=7nm, t_{ox2}=400nm, N_A=10^{16}cm^{-3}.

thin film device the correlation between two MOS gates become more visible.

Analysis of potential profile between the MOS gates of different channel width devices shows that the potential profile remains insensitive to channel width of the device as long as the *cross-sectional* aspect ratio is very low. In Fig. 8(a), both front and back surfaces are kept depleted. It is seen that, for a *cross-sectional* aspect ratio greater than 0.7, the potential profile changes its shape and increases in magnitude.

When the back surface becomes inverted (Fig, 8(b)), the potential profile becomes insensitive to channel width irrespective to *cross-sectional* aspect ratio t_{Si}/L , though potential profile increases in magnitude at the bottom surface end. This is because of the inversion region at the back surface, which is of same type as the junction-gates. The back surface potential gets modulated by the junction-gate biases [3].

The potential distribution along the -direction remains independent of channel length as long as the device aspect ratio W/L remains less than unity but decreases in magnitude for those devices which has aspect ratio greater than unity, as shown in Fig. 8(c).

V. CONCLUSION

The proposed model successfully considers the effects of all four gates and other device parameters. The short channel effect is included in the model by using parabolic assumptions. The proposed model was derived assuming a fully-depleted channel. So, this model perfectly approximates the potential distribution of the body, as the channel remains fully-depleted by the gate biases or if it is already fully-depleted by the combination of channel dimension and doping concentration. With simple modifications, this model can be applied to any of the existing filed-effect transistors e.g. JFET, DGFET etc. as long as the channel is fully-depleted.

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