Journal of Electron Devices, Vol. 11, 2011, pp. 560-566

© JED [ISSN: 1682 -3427]

Journal of Electron Devices
www.jeldev.org

CHARACTERIZATION AND COMPARISON OF LOW POWER SRAM CELLS

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Received 21/09/2011, online 10/10/2011

Abstract

The comparison and analysis of SRAM cells provides vital information for trading of design parameters to meet stringent requirements in the deep sub micron ranges. Initially this paper introduces to SRAM cells, then cell parametric dependences are investigated and finally simulation results of the same are shown. An 11T SRAM cell is compared with the conventional 6T SRAM cell for SNM, Power, DRV and Bit Line capacitances variations. The impact of these parameters variations is investigated in detail and simulations results of the same is discussed.

Keywords: *CMOS; SRAM; SNM; DRV; CR; PR.*

I. INTRODUCTION

In modern integrated chips, SRAM cells occupy a major portion [1]. Now-a-days power dissipation in the memory circuits has become an important design consideration. The advancements in the memory chip require that power consumption during the read and write operations must be low. Technology scaling results in a high density of components but there is a significant increase in leakage current [2]. A minimum size SRAM cell is highly desirable for increasing the memory integration density. As the integration of components increases, leakage power is becoming a prime concern in today's memory chips. Lower voltages and smaller devices cause a significant degradation of data stability in cells [3]. So development of a memory technology with higher stability and lower leakage power consumption characteristics is therefore highly desirable.

In this paper, the 11T SRAM cell [4] reduced power dissipation during both read and writes operations has been discussed. Also leakage power reduction during data-retention in standby SRAM has been analyzed [5]. The two important criteria which have been kept in mind during the implementation of the circuit are non-destructive read operation and reliable write operation. The circuit is implemented and the analysis has been done in 350 nm using the Mentor Graphics Tool, IC Station.

The section II of this paper describes the circuit and working of the 6T & 11T SRAM cell. In section III, various parameters like cell ratio, pull up ratio, data retention voltage, read margin and write margin dependence on SNM have been discussed. Further, in section IV, the comparative power results of 11T SRAM cell and conventional 6T SRAM cell have been discussed.

II. CORE CELL

The two important parameters of SRAM cell are cell current and static noise margin. The static noise margin shows the stability of cell and the cell current decides the delay of cell.

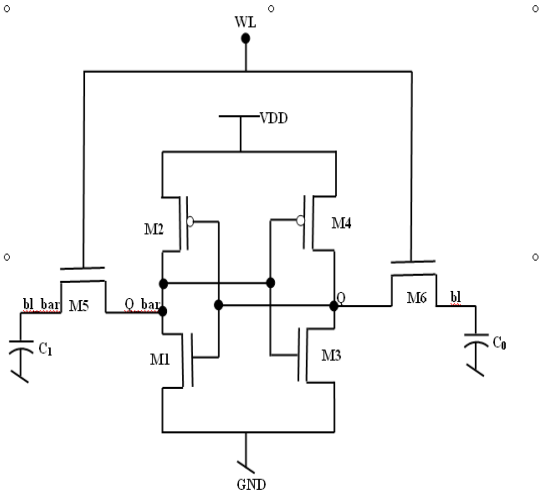

Fig. 1(a). 6T SRAM cell

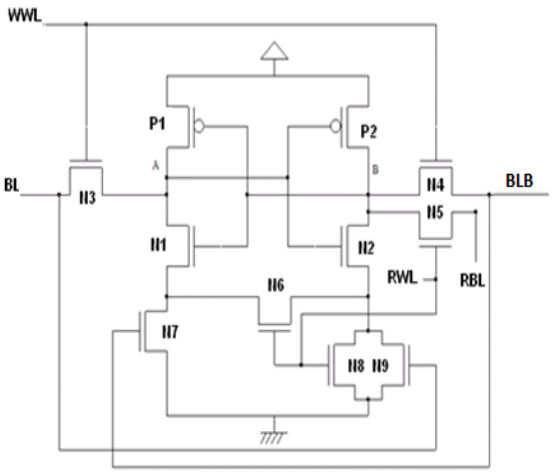

Fig. 1(b). 11T SRAM Cell

II.1 6T SRAM Cell

The conventional SRAM cell consists of two cross coupled CMOS inverters with two access transistors connected to complementary bit-lines. The Figure 1 (a) shows conventional 6T SRAM structure. The gate terminals of both access transistors are connected to the word-line (WL) to perform write operations and the read operations through the column bit lines (BL & BLB). Bit-lines are used to connect SRAM cells to sense-amplifier during read operations and to write circuitry during write operation. The dual bit lines are used to improve noise margins over a single bit line. The symmetric structure in the cell contributes to faster accessing a memory location. The careful sizing of the transistors is done by considering cell ratio (CR), pull-up ratio (PR), static noise margin (SNM) [6] and layout symmetry for proper operation of SRAM cell. This cell has been found to be unstable at deep sub-micron technology due to a low read SNM, high power dissipation, low read margin and write margin. These issues have been improved by adding additional transistors to the original 6T cell.

II.2 11T SRAM Cell

An 11T SRAM cell is shown in Figure 1(b). The implemented circuit consists of 11 transistors instead of just 6 as in conventional SRAM cell. Due to lesser power dissipation of the 11T SRAM cell, the area overhead of the cell can be tolerated. The circuit consists of two cross coupled inverters along with an access transistor (N5) which is controlled by the read word line (RWL) for read operation and two more access transistors (N3 and N4) which are controlled by the write word line (WWL) for write operation. The two other NMOS transistors, N6 and N8 are used during the read operation to reduce power dissipation while NMOS transistors, N7 and N9 are used during the write operation to reduce power dissipation of the cell. The two tail transistors, N7 and N9 are controlled by the bit lines, BLB and BL, respectively while the read operation uses a single bit line RBL.

II.2.1 Read Operation

During the read operation there is no need to assert the WWL. For read operation RWL is turned ON. Now, either read1 or read 0 operations can be performed depending on the data stored at node B. The output of the read operation is taken through the bit line RBL. In 11T SRAM cell, a lot of power is saved as no bit line discharges during the read operation. The simplified model of the 11T SRAM cell during the read operation is shown in Figure 2(a).

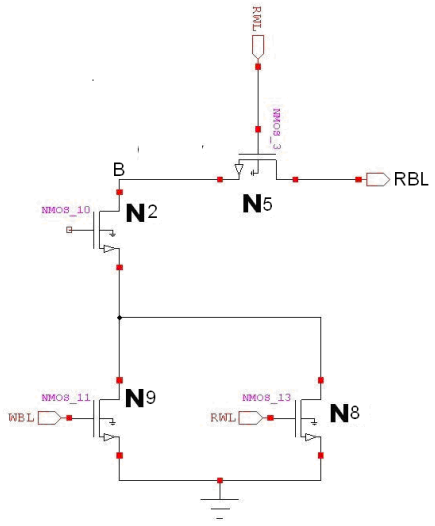

Fig. 2 (a). Simplified Circuit during Read Operation

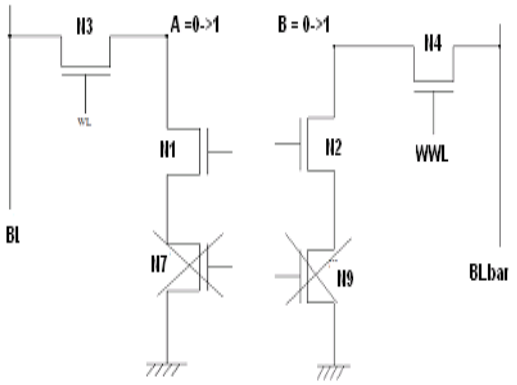

Fig. 2 (b). Simplified Circuit during Write Operation

II.2.2 Write Operation

The write operation is performed using the write word line WWL and the read word line RWL can be set to value zero. Depending on whether write '0' or write '1' operation is to be performed, appropriate value of bit lines BL and BLB is selected. The simplified model of 11T SRAM cell during the write '0' and write '1' operations is shown below in Figure 2(b). In both the operations, write '0' and write '1' neither BL or BLB is charging nor discharging, that's why a lot of power is saved during write '1' and write '0' operations.

III. SNM DEPENDENCES

The SRAM cell immunity to static noise is measured in terms of SNM. The maximum amount of voltage noise that can be tolerated at cross-inverters output without flipping the cell. It is the measure of the stability of the cell. SNM is key performance factor during read and hold operations. During read operation SNM takes its lowest value and the state of cell is weakest. The value of SNM depends on the CR, PR and supply voltage [7]. In this paper, SNM is calculated by the traditional Butterfly method.

In this section, the simulation results of 11T SRAM Cell for Static Noise Margin is calculated by varying parameters like CR, PR, DRV, RM and WM. They have been compared with the results of the conventional 6T SRAM cell. All the analysis has been performed on 350 nm technology. Also, the results for power analysis of 11T SRAM cell in comparison with 6T SRAM cell have been done.

III.1 Cell Ratio (CR) vs. Static Noise Margin (SNM)

The SNM improvements using the transistor width modulation technique is computed during read operation [8]. The cells are designed to provide a non-destructive read operation and a reliable write operation. The transistor sizing is done in the cell to satisfy both the conditions according to the CR and PR. Table 1 presents the SNM variation of both 6T & 11T SRAM cell with the cell ratio (CR) during the read operation. It can be seen that as the CR of the SRAM cell increases, the SNM also increases [9]. Also, the SNM of 11T SRAM cell is greater than that for 6T SRAM cell for the same value of CR. This means 11T SRAM cell is more stable.

Table 1: SNM variation with CR

Cell Ratio (CR)	SNM (mV) 11T SRAM	SNM (mV) 6T SRAM
0.6	271	100
0.8	280	102.5
1.0	291	104.6
1.2	299	107
1.4	308	108
1.6	319	112
1.8	334	116.7
2.0	340	123

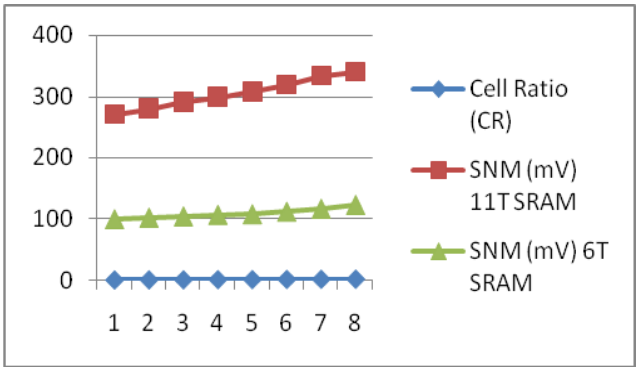

Figure 3: Cell Ratio (CR) vs. Static Noise Margin (SNM)

In Figure 3, the SNM variations of 6T and 11T SRAM cell with Cell Ratio is shown. It can be concluded from the graph that the noise tolerance of 11T SRAM cell is more. This is because CR is directly proportional to the width of driver transistor and the driver transistor has the maximum effect on static noise margin.

III.2 Pull up Ratio (PR) vs. Static Noise Margin (SNM)

Table 2 presents the SNM variation of both 6T & 11T SRAM cell with the pull up ratio (PR) during the write operation [15]. It can be seen that as the PR of the SRAM cell increases, the SNM also increases. Also, the SNM of 11T SRAM cell is greater than that for 6T SRAM cell for the same value of PR. This means 11T SRAM cell is more stable. In Figure 4, the profile of the write SNM variation with pull up ratio for both 11T SRAM cell and 6T SRAM cell is shown.

Table 2: SNM variation with PR

Pull Up Ratio (PR)	Write SNM (mV) 11T SRAM	Write SNM (mV) 6T SRAM
1.05	241	92.9
1.2	242	94
1.4	244	94.6
1.6	246	95
1.8	249	95.5
2.0	250	96
2.1	251	96.7
2.2	253	97.8
2.4	257	99.2
2.6	259	100.4
2.8	260	102.3
3.0	262	104

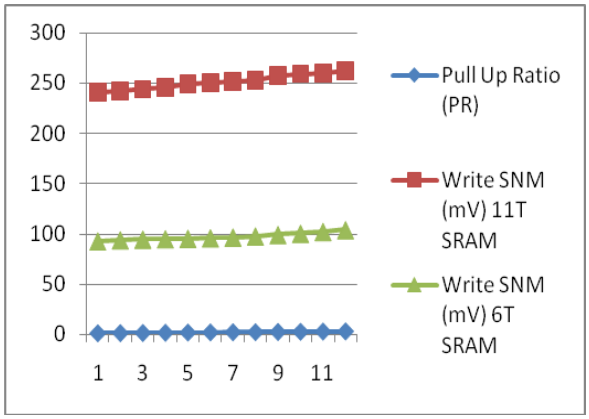

Figure 4: Pull Up Ratio (PR) vs. Static Noise Margin (SNM)

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The SNM gain is higher when increasing CR ratio than when increasing only the PR ratio. Although increasing both CR & PR provides significant higher SNM improvements. But increasing these will results in higher leakage currents and inturn that results in higher power dissipation.

III.3 Data Retention Voltage (DRV) vs. Static Noise Margin (SNM)

The static power consumption can be minimized by lowering power supply voltage to standby [10]. The minimum supply voltage required for non-zero static noise margin is calculated using conventional butterfly curve . Table 3 presents the variation of static noise margin for both 11T and 6T SRAM cells with the variation in supply voltage. As the supply voltage is reduced the static noise margin of the SRAM cell. For the same value of V_{dd}, SNM of 11T SRAM cell is greater than that of 6T SRAM cell.

Table 3: SNM variation with Supply Voltage (V_{dd})

Power Supply (VDD) (in Volts)	SNM (mV) 11T SRAM	SNM (mV) 6T SRAM
2.3	187	95.2
2.1	166	82
1.8	148	74.6
1.5	129	62.1
1	113	53
0.8	100	44
0.6	70	32.3
0.5	32	24.7
0.4	0	10.9
0.3	0	0

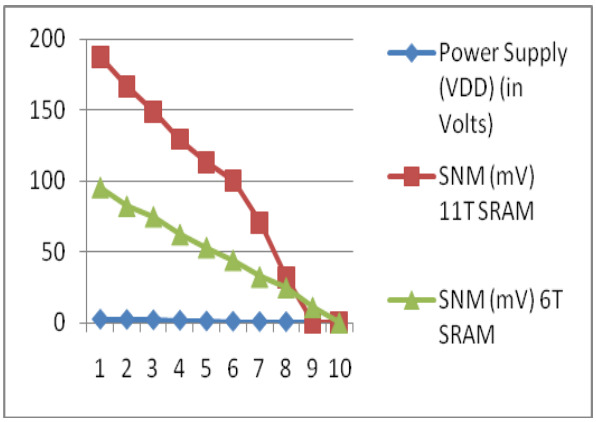

Figure 5: DRV vs. SNM

Figure 5 shows the variation of SNM with Supply Voltage (V_{dd}). For 6T SRAM cell, DRV is 0.3V and for 11T SRAM cell DRV is obtained at 0.4V.

IV. POWER ANALYSIS

The SRAM cell power consumption is majorly depends on the transistor widths, threshold voltages of transistors [11], supply voltage and bit line capacitances. Transistor sizing for enhanced data stability comes at the cost of leakage power [12]. In this section, the power analysis of 11T SRAM cell has been done by varying parameters like Temperature, Supply voltage, capacitance and frequency. The results have been compared with that of the conventional 6T SRAM cell. The power analyzed here is the average power which consists of both static and dynamic power [13] [14].

4.1 Temperature vs. Power Dissipation

Table 6 presents the variation of power dissipation with temperature for both 6T SRAM cell and 11T SRAM cell. It is observed that the power dissipation of 11T SRAM cell is much lower than that for 6T SRAM cell for the same value of temperature shown in Figure 6.

Table 6: Variation of Power dissipation with Temperature

Temperature (^{0}C)	6T Cell Power Dissipation (pw)	11T Power Dissipation (pw)
0	66.5688	39.5402
5	66.9243	40.2024
10	67.4591	41.0517
15	68.0234	42.1322
20	68.8615	43.5032
25	69.7287	45.3026
27	70.5036	46.1243
30	72.9018	47.5201
35	76.0813	50.3854
40	80.9964	54.1782
45	84.2878	59.3794
50	89.2715	66.8385

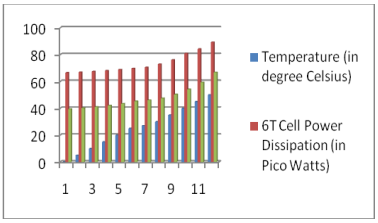

Figure 6: Power Dissipation Vs Temperature

IV.2. Supply Voltage (V_{dd}) vs. Power Dissipation

Table 7 presents the variation of power dissipation with supply voltage. Since, the dynamic power is directly proportional to the square of supply voltage, so as the supply voltage is reduced, the power dissipation also decreases.

Table 7: Variation of Power dissipation with Supply Voltage

Supply Voltage (Vdd in Volts)	6T Cell Power Dissipation (in Pico Watts)	11T Power Dissipation (in Pico Watts)
5.0	396.5366	68.4357
4.5	340.8164	64.7294
4.0	274.1283	59.6143
3.5	196.2356	55.6481
3.0	129.9901	50.0972
2.5	70.5036	46.1243
2.0	67.3492	42.6591
1.5	59.5460	37.2356
1.0	51.4837	32.8437
0.5	46.8218	26.3189

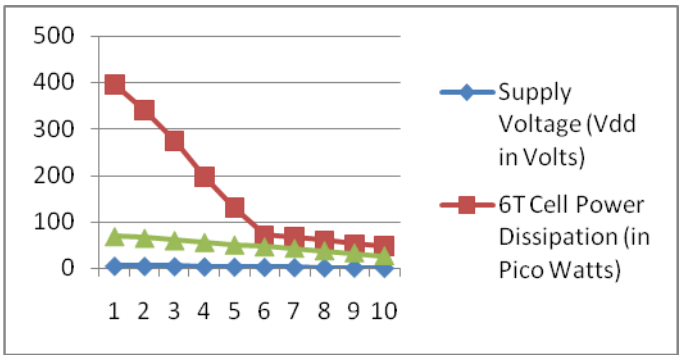

Figure 7: Power Dissipation vs. Supply Voltage

Figure 7 shows the variation of power dissipation with supply voltage. The power dissipation in 6T cell is higher compared to 11T cell.

IV.3. Capacitance vs. Power Dissipation

The bit-line capacitances plays crucial role in power dissipation during the read and write operation. For the read operation, differential voltage required on bit line and in write operation, discharging of bit line voltage is required. Table 8 presents the variation of power dissipation with bit line capacitance. Since, dynamic power dissipation is directly proportional to the capacitance, its value increases with increasing capacitance. The power dissipation of the 11T SRAM cell is much lower than that of the 6T SRAM cell for the same value of capacitance. The analysis has been done at a fixed frequency of 100 MHz.

Table 8: Variation of Power dissipation with Capacitance

Capacitance (pf)	6T Cell (pw)	11T Cell (pw)
5.0	267.900	209.4
4.0	240.1985	167.9
3.0	213.3276	125.2
2.0	198.8266	103.7
1.5	174.240	85.1
1.0	139.428	69.3
0.8	118.4567	61.5
0.5	99.6709	55.08
0.1	70.5	46.2

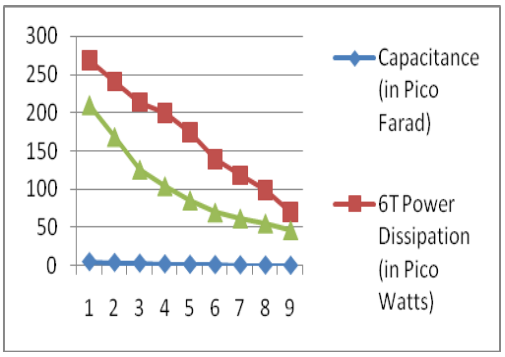

Figure 8: Power Dissipation vs. Capacitance

Figure 8 shows the graph for variation of power dissipation with capacitance.

IV.5. Frequency vs. Power Dissipation

Table 9 presents the variation of power dissipation with frequency. Since, dynamic power dissipation is directly proportional to the frequency, its value increases with increasing frequency. The power dissipation of the 11T SRAM cell is much lower than that of the 6T SRAM cell for the same value of capacitance. The analysis has been done at a fixed capacitance of 0.1pf.

Table 9: Variation of Power dissipation with Frequency

Frequency (in MHz)	6T Cell (pw)	11T Cell(pw)
150	124.0915	69.5634
140	116.6790	62.7825
130	110.4321	56.2719
120	103.6098	51.4637
110	91.7689	46.1243
100	70.5036	43.5032
90	76.4382	42.6732
80	69.579	39.5402
70	61.4656	36.7963
50	55.3912	33.2745

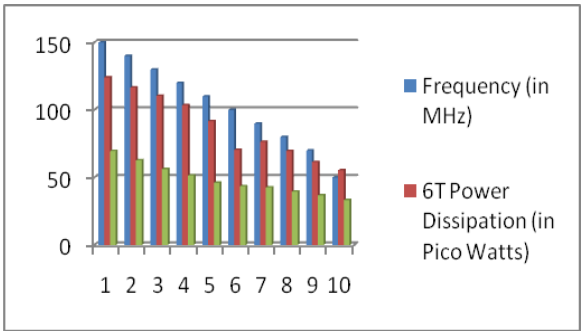

Figure 9: Power Dissipation vs. Frequency

Figure 9 shows the bar graph for the variation of power dissipation of 6T and 11T SRAM cell with frequency.

V. CONCLUSION

From the Static Noise Margin (SNM) Analysis, it can be concluded that the 11T SRAM cell has a higher SNM than the conventional 6T SRAM cell, i.e. 11T SRAM cell has a greater noise tolerance. Also, from the power analysis it can be seen that 11T SRAM cell has lower power dissipation in both read and write operations than the 6T SRAM cell. The only drawback over the 6T SRAM cell is the area overhead of the 11T SRAM cell.

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