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TRANSIENT AND DELAY ANALYSIS FOR ON-CHIP HIGH SPEED VLSI RLCG INTERCONNECTION NETWORK IN 0.18µm TECHNOLOGY

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Abstract— In this paper, the time domain waveform is approximated for calculation of delay, rise, settling time, damping ratio and natural frequency of a second order RLCG on-chip VLSI interconnect line. It can also be evaluated for multiple interconnect systems but due to harmonics higher order systems are ignored. The model is applied to a single RLCG interconnect line which can also be extended for multi-interconnect systems to analyze crosstalk noise. The model evaluates the performance of a system which is expressed in terms of the transient response due to a unit step input. It is easy to generate and evaluate the delay analytically. A closed form expression for the propagation delay of a CMOS gate driving a distributed RLCG line is introduced. On-chip inductance and conductance are expected to have a profound effect on traditional high performance IC design methodologies. In the proposed model, it is shown that when the value of G is increased, the time at which the rise time, settling time and the time when the steady state condition is reached are all increased. So, for high speed circuits one must increase the value of G so that the steady state condition is reached quickly and it is also shown that with the increase in the value of G the delay will reduce. The simulation results performed in SPICE environment justify the efficacy of the proposed model.

Keywords- Time Domain Analysis, Damping Ratio, Natural Frequency, Delay Calculation, RLCG Interconnect, VLSI.

I. INTRODUCTION

The design techniques in sub-micron technologies results in increase in coupling in interconnections. As integrated circuit's feature size continues to scale well below 0.18 microns [1], active device counts are reaching hundreds of millions. The amount of interconnects among the devices tends to grow super linearly with the transistor counts, and the chip area is often limited by the physical interconnect area. In deep sub micrometer integrated circuits, interconnect delay dominates gate delay. In the present day VLSI technology, the wire inductance can no longer be ignored, due to higher signal frequencies and longer wire lengths. The transient time [2] is the time between zero to the steady state value at which the system is operating. In this RLCG network, we evaluate the delay by using an analytical approach; the delay is directly evaluated from $t_{plh}/2$. Generally in cases when high frequencies are considered, no insulator can act like a perfect insulator (as typically considered as ideal), thus there is always a probability of leakage, and conductance is considered as a measure of this leakage. With the increase in speed of high performance VLSI circuits, inductance and conductance effect of interconnects are becoming more and more important and can no longer be neglected. Under these circumstances, the Elmore model [3] is inadequate since this model takes only the resistance and capacitance effects into account. It is necessary to use a second order model, which includes the effect of inductance and conductance. There are several approaches proposed to estimate the on-chip interconnect performance characteristics; where the interconnect is modelled as distributed RC [4-5], RLC [6-9], and RLCG segment [10-14].

The following contributions have been made in this paper: a closed form expression for delay metric for on-chip VLSI interconnect using distributed RLCG model has been proposed.

The rest of the paper is organized as follows: basic theory of transmission line when considered as a distributed RLCG model is discussed in section 2. Section 3 discusses on the unit impulse function which is considered as an input for the on-chip interconnect delay calculation. Proposed transient response and delay model of RLCG interconnection network is given in section 4. Simulation results are shown and discussed in section 5 and finally section 6 concludes the paper.

II. BASIC THEORY

II.1 Transmission Line Model

Defining the point at which on-chip interconnect should be treated as a transmission line and hence reflection analysis applied has no consensus of opinion. A rule of thumb is when the delay from one end to the other is greater than risetime/2, the line is considered as electrically long, if the delay is less than risetime/2, the line is said to be electrically short [15].

A transmission line can be described at the circuit level using series inductance and resistance combined with shunt capacitance and conductance [16]. An infinitesimal unit length of the transmission line circuit is shown in Figure 1.

In Figure 1, R = series resistance per unit length; L = series inductance per unit length; G = shunt conductance per unit length; C = shunt capacitance per unit length.

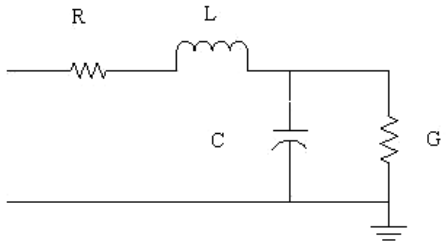

Figure 1. RLCG Segment of a Transmission Line

It is critical to model the transmission path when designing a high-performance, high-speed serial interconnect system. The transmission path may include long transmission lines, connectors, vias and delay from adjacent interconnects.

II.2 Impulse Function

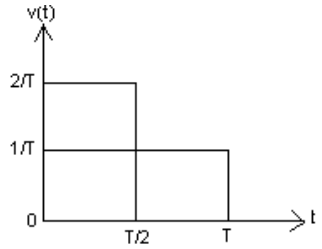

Figure 2. Impulse Response Representation

In Figure 2, the first pulse has a width T and a height of 1/T such that the area of the pulse is T×1/T=1. If we halve the duration and double the amplitude we get the second pulse. The area under the second pulse is also unity. Note that the duration of the pulse approaches infinity but the area of the pulse is unity. The pulse for which the duration tends to zero and amplitude tends to infinity is called impulse function. Impulse function is also known as delta function,

A unit impulse can be defined as,

$$\delta(t)=\begin{cases}0;t\neq 0\\ \infty;t=0\end{cases} \tag{1}$$

III. PROPOSED DELAY MODEL

We have obtained an analytical delay model, based on the time domain analysis of RLCG interconnection lines, which considers the effect of conductance. An analytical delay model has been proposed for RLC interconnect [7] does not consider the effect of shunt conductance in interconnect modelling. The exact transfer function of a widely used interconnect model [16] is described in this section and a time domain analysis of a typical on-chip signal is done and is represented by the interconnection network which is being evaluated for 0.18 μm technology. An interconnect model is shown in Figure 3. An interconnects represented by a distributed RLCG transmission line, where R, L, C and G are the resistance, inductance, capacitance and conductance per unit length. The load of the interconnect is modelled as a conductance.

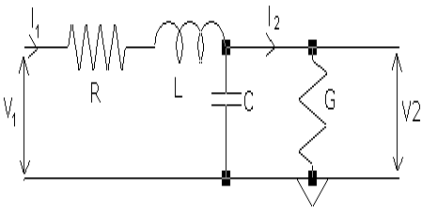

Figure 3. Equivalent circuit model for an RLCG distributed interconnect.

By applying Kirchhoff's voltage law in the network, we can write,

$$V_1 = i_1R + i_1sL + (i_1\text{-}i_2)\frac{1}{sC} \tag{2}$$

$$\text{-}i_2\cdot\frac{1}{G}\text{-}(i_2\text{-}i_1)\frac{1}{sC}=0 \tag{3}$$

$$V_2 = i_2\cdot\frac{1}{G} \tag{4}$$

By solving the above three equations (2-4), we obtain the open loop transfer function as,

$$G(s)=\frac{V_2}{V_1}=\frac{\frac{1}{LC}}{s^2+\frac{(RC+LG)}{LC}s+\frac{(RG+1)}{LC}} \tag{5}$$

Consider the time response of second order system, where we consider the closed loop transfer function which can be written as,

$$\frac{V_2}{V_1}=\frac{G(s)}{1+G(s)H(s)}=\frac{\omega_n{}^2}{s^2+2\zeta\omega ns+\omega_n{}^2} \tag{6}$$

$$v_2(s)=\frac{\omega_n{}^2}{s^2+2\zeta\omega_n s+\omega_n{}^2}v_1(s)$$

For unit step input,

$$R(s)=\frac{1}{s} \tag{7}$$

$$C(s)=\frac{1}{s}\left(\frac{\omega_n{}^2}{s^2+2\zeta\omega_n s+\omega_n{}^2}\right) \tag{8}$$

Replacing the term ($s^2+2\zeta\omega_n{}^2+\omega_n{}^2$) by

$(s+\zeta\omega_n)^2+\omega_n{}^2(1-\zeta^2)$ in (8), we get

$$C(s)=\frac{1}{s}\left(\frac{\omega_n{}^2}{(s+\zeta\omega_n)^2+\omega_n{}^2(1-\zeta^2)}\right) \tag{9}$$

After partial fraction the above equation can be written as,

$$C(s)=\frac{1}{s}-\frac{s+2\zeta\omega_n}{(s+\zeta\omega_n)^2+\omega^2{}_d} \tag{10}$$

where $\omega^2{}_d=\omega^2{}_n(1-\zeta^2)$

Taking Laplace inverse of equation (10), we get,

$$C(t) = 1 - \left[e^{-\zeta\omega_n t}.\cos\omega_d t + \frac{\xi\omega_n}{\omega_d} e^{-\zeta\omega_n t}.\sin\omega_d t \right] \quad (11)$$

By substituting $\omega^2{}_d = \omega_n\sqrt{(1-\zeta^2)}$; $\phi = \zeta, \tan\phi = \frac{\sqrt{1-\zeta^2}}{\zeta}$ in (11),

$$C(t) = 1 - \frac{e^{-\zeta\omega_n t}}{\sqrt{1-\zeta^2}}\left[\sin\phi.\cos\omega_d t + \cos\phi.\sin\omega_d t\right] \quad (12)$$

After simplification we can write,

$$C(t) = 1 - \frac{e^{-\zeta\omega_n t}}{\sqrt{1-\zeta^2}}(\sin\omega_d t + \phi) \quad (13)$$

After putting the values of $\omega_d and \phi$ in equation (13),

$$C(t) = 1 - \frac{e^{-\zeta\omega_n t}}{\sqrt{1-\zeta^2}}\sin\left[\left(\omega_n\sqrt{1-\zeta^2}\right)t + \tan^{-1}\frac{\sqrt{1-\zeta^2}}{\zeta}\right] \quad (14)$$

The error signal for the system can be written as,

$e(t) = r(t) - c(t)$

$$e(t) = \frac{e^{-\zeta\omega_n t}}{\sqrt{1-\zeta^2}}\sin\left[\left(\omega_n\sqrt{1-\zeta^2}\right)t + \tan^{-1}\frac{\sqrt{1-\zeta^2}}{\zeta}\right] \quad (15)$$

The steady state value of $c(t)$ is

$$e_{ss} = \lim_{t\to\infty} c(t) = 1 \quad (16)$$

At steady state there is no error between input and output, so the characteristic equation for this transfer function can be written as,

$$1 + G(s)H(s) = 0 \quad (17)$$

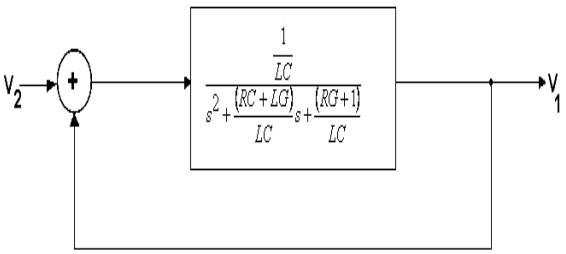

Figure 4. Block diagram of second order system

For unity feedback system (as shown in the Figure 4) and the unit step input, (17) can be written as,

$$1 + G(s) = 0 \quad (18)$$

Using (5), the characteristic equation can be written as,

$$1 + \frac{1}{s^2 + \frac{(RC+LG)}{LC}s + \frac{(RG+1)}{LC}} = 0 \quad (19)$$

After simplifying the characteristic equation for a unity feedback system can be written as,

$$s^2 + \frac{(RC+LG)}{LC}s + \frac{(RG+2)}{LC} = 0 \quad (20)$$

Now comparing the characteristic equation of second order system with unity feedback with (20), we obtain the values of ω_n and ζ which are the natural frequency and damping ratio, respectively.

$$\omega_n = \sqrt{\frac{RG+2}{LC}} \quad (21)$$

$$\zeta = \frac{\frac{RC+LG}{LC}}{2\sqrt{\frac{RG+2}{LC}}} \quad (22)$$

IV. SIMULATION RESULTS AND DISCUSSIONS

The high-speed interconnect system consists interconnect line as shown in Figure 3 and ground; the length of the lines is d =100 µm. The extracted values for the parameters R, L, C, and G are given in Table 1. The Sample dimension of cross-sections of minimum sized wire in a 0.18µm technology is shown in Figure 5. By substituting the values of RLCG for 0.18 micron technology in the proposed delay model we obtain the various parameters which are required to synthesize the interconnection network. In the transient analysis, we consider a closed loop system for a unit impulse input. The Table II given below shows the values of the R, L, G, C, ω_n, ζ and delay (t_d) by which we obtain an closed loop response of a LTI system. These parameters are very useful for analysis of any system and evaluating the response of that system. This analytical model evaluates the performance of high speed interconnection network by calculating the delay.

TABLE I. RLCG PARAMETERS FOR A MINIMUM-SIZED WIRE IN 0.18 MICRON TECHNOLOGY

Parameter(s)	Value/m
Resistance(R)	120 kΩ/m
Inductance(L)	270 nH/m
Conductance(G)	15f pS/m
Capacitance(C)	240 pF/m

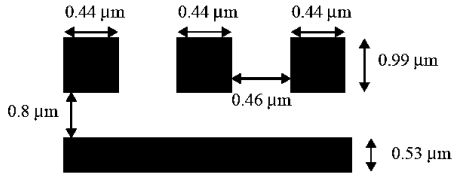

Figure 5. Sample Dimensions of Cross-sections of minimum sized wire in a 0.18µm technology

The delay is calculated by evaluating the rise time of a linear time invariant system. This model also evaluates the settling time, maximum overshoot, and maximum amplitude of the LTI system. We have obtained an analytical delay model, based on the time domain analysis RLCG interconnection lines, which considers the effect of conductance. Table II shows that with the increase in the value of G the delay will reduce in proposed delay model (t_{dp}) and similarly it is being compared with the

delay model of SPICE (t_{ds}) that will also being evaluated and shown that with the increase in the value of G the delay will reduce.

TABLE II. COMPARISON BETWEEN PROPOSED DELAY MODEL AND SPICE DELAY MODEL

R (KΩ)	L (nH)	C (pF)	G (mS)	ω_n rad/sec (10^{10})	ζ	Proposed delay t_{dp}(ns)	Spice Delay T_{ds} (ns)
1.2	2.7	2.4	1.5	2.42	9.19	3.0	3.22
1.2	2.7	2.4	2.25	2.69	8.27	2.25	2.51
1.2	2.7	2.4	3	2.93	7.60	1.50	1.71
1.2	2.7	2.4	3.75	3.15	7.07	1.25	1.49

Table I shows the value of RLCG under 0.18micron technology, ω_n defines the natural frequency, ζ is the damping ratio, t_{dp} is the delay calculated using proposed model and t_{ds} is the delay calculated using SPICE. Table III shows the delay calculated using t_p, t_s, where t_p is the time to reach to the peak amplitude and t_s is settling time. t_d is the delay calculated using the proposed delay model t_{d1} is the delay calculated for the proposed model using SPICE.

TABLE III. THE TIME- DOMAIN MODEL PARAMETERS.

R (KΩ)	L (nH)	C (pF)	G (mS)	Peak amplitude time t_p (ps)	Settling time t_s (ns)	delay t_d(ps)
1.2	2.7	2.4	1.5	14.3	2.98	3.57
1.2	2.7	2.4	2.25	12.0	2.41	3.00
1.2	2.7	2.4	3	11.9	2.04	2.97
1.2	2.7	2.4	3.725	11.2	1.76	2.80

All these analysis are being carried out by using time domain parameters and the values of R, L, C, G in the network. In MATLAB, we evaluate the rise time (t_r), settling time (t_s) and it is shown in Table IV that when the value of G is increased, the rise time and settling time will reduce, hence the delay, denoted by t_d, will also be reduced. Fig. 6 shows unit impulse response for a closed loop LTI system for various values of ζ and ω_n. Similarly Fig. 7 shows the unit step response for a closed loop LTI system. Figs. 8-11 show the SPICE output for the given RLCG network. From which the delay can be evaluated for the same parameters as shows in Table I.

TABLE IV. THE TIME- DOMAIN MODEL PARAMETERS FOR STEP INPUT

R (KΩ)	L (nH)	C (pF)	G (mS)	t_r (ns)	t_s (ns)	t_d (ns)
1.2	2.7	2.4	1.5	1.66	2.96	2.25
1.2	2.7	2.4	2.25	1.35	2.4	2.00
1.2	2.7	2.4	3	1.14	1.14	1.75
1.2	2.7	2.4	3.725	.982	1.75	1.50

In Figures 8-11, it is shown that by increasing the value of G with constant RLC values the delay will reduce for a linear time invariant system for step input.

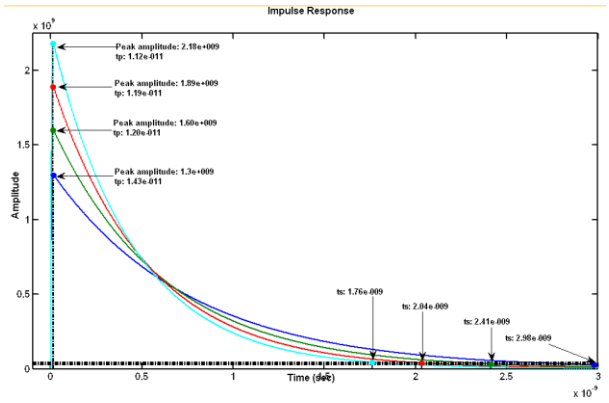

Figure 6. Transient response of a Linear time invariant system for unit impulse input.

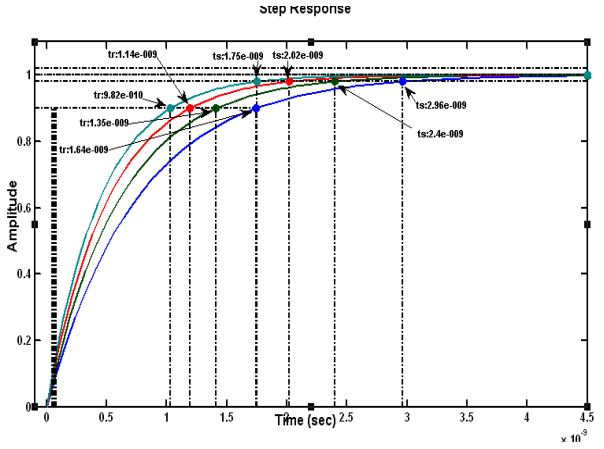

Figure 7. Transient response of a Linear time invariant system for unit step input.

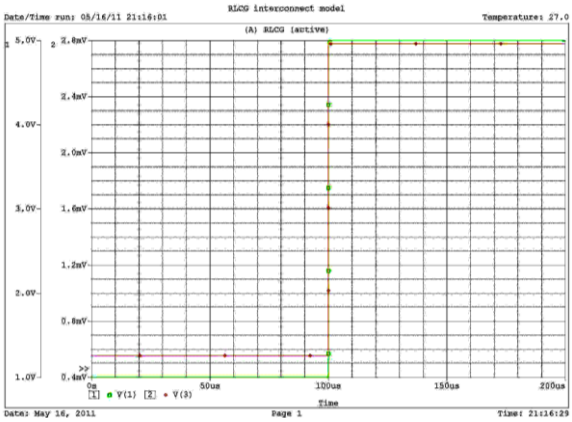

Figure 8. A Spice model for delay calculation in RLCG network for the values R(KΩ)=1.2, L(nH)=2.7,C(pF)=2.4 and G(mS) =1.5 in a 0.18µm technology.

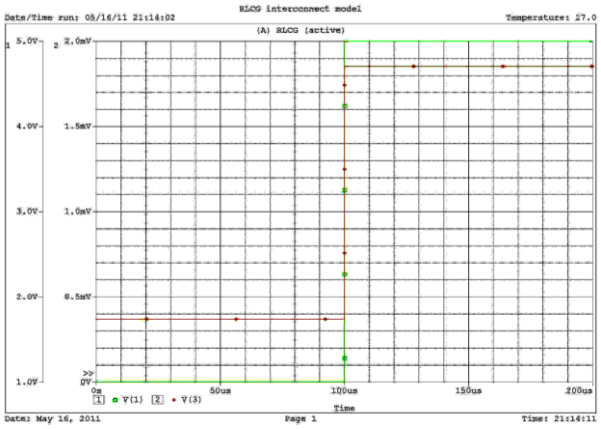

Figure 9. A Spice model for delay calculation in RLCG network using values R(K**Ω**)=1.2, L(nH)=2.7, C(pF)=2.4 and G(mS) =2.25 in a 0.18µm technology.

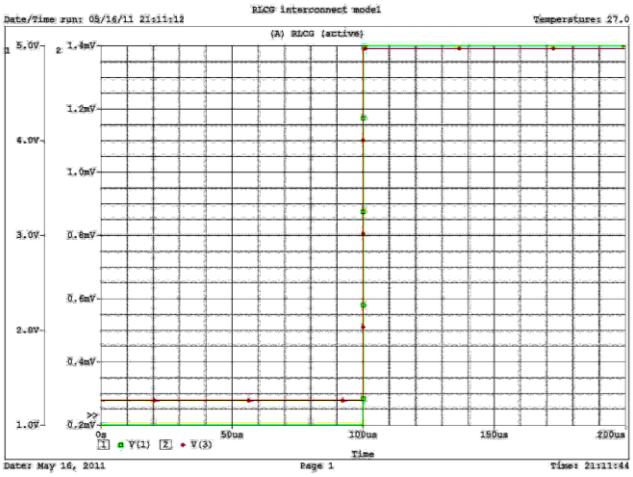

Figure 10. A Spice model for delay calculation in RLCG network using values R(K**Ω**)=1.2 ,L(nH)=2.7,C(pF)=2.4 and G(mS) =3.0 in a 0.18µm technology

In Figure 8, the delay is evaluated using spice as t_{d1} =0.52 ns with the values of RLCG shown above. In this figure the delay is large by comparing the other figures. In Figure 9, we evaluated the delay using spice as t_{d1} =.51ns by using the values of RLCG shown above. In this Figure 9 the delay is reduced by comparing the other Figure 8.

In the above shown Figure 10 we evaluate the delay using spice as t_{d1} =0.50 ns by using the values of RLCG shown above. In this figure the delay is reduced by comparing the other Figure 9 and 10.

In the above shown Figure (11) we evaluate the delay using spice as t_{d1} =0.49ns by using the values of RLCG shown above. In this fig the delay is reduced by for large value of G so in these SPICE calculations we see that by increasing the value of G the delay is reduced by comparing the other figures of Spice.

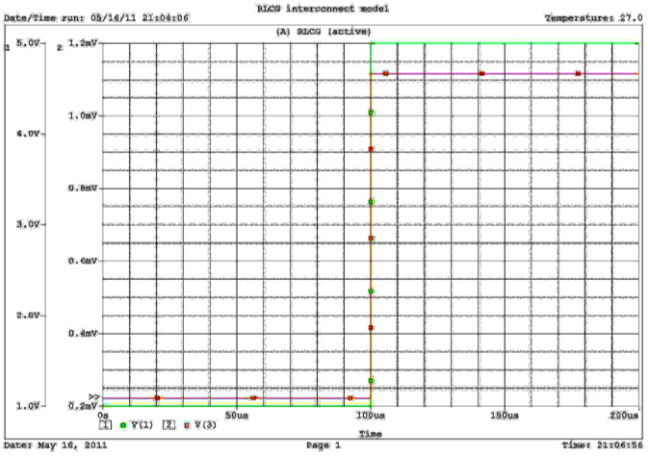

Figure 11. A Spice model for delay calculation in RLCG network using values R(K**Ω**)=1.2, L(nH)=2.7,C(pF)=2.4 and G(mS) =3.725 in a 0.18µm technology

V. CONCLUSION

We have proposed an analytical delay model shown in the block diagram of the second order control system, which considers the effect of conductance. The resulting delay estimates are significantly more accurate in comparison to other delay model and it will evaluate the performance of this interconnection network by increasing the value of conductance when the delay is reduced. The derived expression along with the analysis can serve as a convenient tool for delay estimation without much computation during design. Simulation results demonstrate the validity and correctness of our proposed model. It is also shown that when the value of G is increased the time, at which the rise time, settling time and steady state condition is reached, is increased. So, for high speed circuit, the value of G is as high as possible so that the steady state condition is reached as soon as possible. It is also demonstrated that with the increase of G the delay will also be reduced.

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