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A NOVEL CIRCUIT REDUCTION TECHNIQUE TO DETERMINE THE RESPONSE OF THE ON-CHIP VLSI RC INTERCONNECT FOR RAMP INPUT EXCITATION

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Abstract- In present day sub-micron technology, reduction of circuit complexity of on-chip VLSI interconnects is an important issue for the analysis and verification of integrated circuits. In this paper, we present an exact method to compute the analytic time-domain response for a RC circuit including coupling capacitors for ramp input excitation. Accuracy and efficiency of the method is shown for various examples.

Key words: RC Interconnect; VLSI; Reduction Technique; Execution Time; Circuit Complexity; Ramp Input

I. INTRODUCTION

In deep sub-micron VLSI technology, parasitic elements play an important role in the analysis of on-chip VLSI interconnects. These parasitic elements arise mainly due to the increased number of metal level, thinner metal width, increased wire height versus width ratio and smaller wire spacing. Interconnects are hereby modelled as RC circuit as shown in Figure 1.

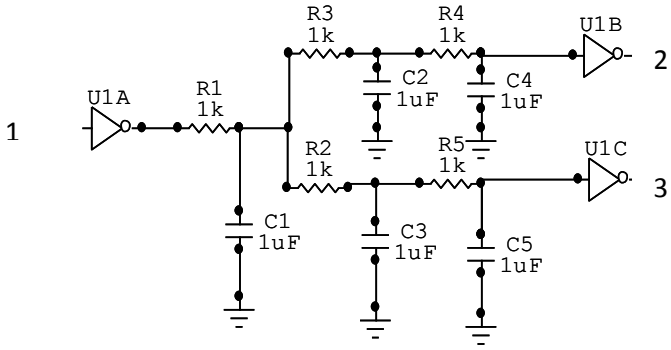


Fig.1. Example of RC Circuit (All Resistors have the value *R* and all Capacitors have the value *C*)

There exists some coupling capacitance which can be added between two neighbouring wires (Figure 2).
The set of RC elements used to model the wire is known as RC network. These networks can have two significant impacts on the on-chip VLSI circuits: timing and functional failure. When the output of gate 1 makes a transition, a current is injected through the coupling capacitance on the interconnection located between gates 4 and 5. If the gate 4 is making a transition, the injected current can accelerate or decelerate the transition which in turn results in the timing failure. If the gate 4 is in the steady state, the injected current can generate a noise, which can produce a functional failure if it is not rapidly absorbed by the emitter 4. Nowadays, these parasitic elements can no longer be neglected and must be taken into account in the design methodologies, design and verification tools. [2] and [10] propose some methodologies to reduce the impact of parasitic elements. New place and route tools are developed in order to take the crosstalk phenomenon into account. The model presented in [1] proposes a new global timing placement. [12] presents an algorithm to solve crosstalk violation elimination problem and in [4], a technique is presented considering the river routing crosstalk constraints. Motivated by the circumstance, [13] presents a method to capture crosstalk induced noisy waveform for static timing analysis. Several methods have been proposed to evaluate the crosstalk noise in the on-chip RC interconnect circuit with crosstalk coupling capacitance [3] [8-9] [18-21]. These methods are quite simpler but suffer from a lack of accuracy.

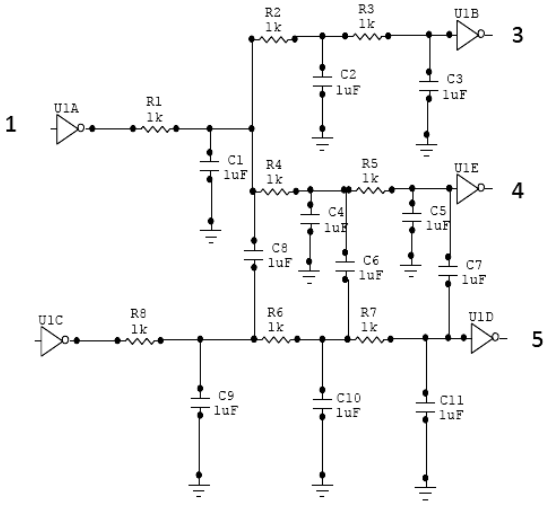


Fig.2. Example of RC circuit with Coupling Capacitance (All Resistors have the value R and all Capacitors have the value C)

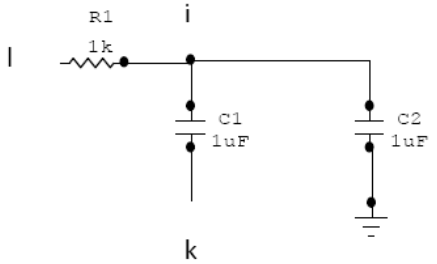
In order to capture the actual performance of the real size on-chip interconnect circuit, the RC circuits can comprise of a number of parasitic elements (nearly 1000 to 10,000 resistances and ground capacitors) and have a complex topology with crosstalk coupling capacitors. Thus the parasitic RC circuits can not be directly taken into account in verification tools. In this paper, we propose a method to

reduce the complexity of the RC interconnect circuit analysis by reducing the order of the RC network. The reduction consists of the modelling of the original RC circuit with a smaller number of elements while still maintaining the circuit's characteristics. This has been an area of considerable research over the last few years [1] [6-7] [14-16]. The methods proposed by Elmore [1] in 1948 and modified by Rubinstein *et al.* [7] propose to estimate the 50% propagation delay for RC tree without coupling capacitance. This method can not be easily extended to capture the propagation delay for RC network with coupling capacitance. Recently, the AWE method [11] and its derivative, the first three moments method [6] provide an approximated expression of a RC network output. In matching the first *n* moments (*n*=3 [6]) of the impulse response shows that these methods can generate a significant amount of error when the analysis is extended with the coupling capacitance. In addition, it is well known that AWE can be unstable. The PVL [15] and PRIMA [16] methods are proposed, to match the first *n* moments of the RC networks with different mathematical formulations. Due to the complexity of these methods and due to the difficulty of finding the number of moments which give a satisfying accuracy / computation time ratio, it is really difficult to use these methods. The model proposed in [17] deals with the RC circuit reduction for step input. But in actual practice the input signal does have a definite finite rise/ fall time. In this paper, the same approach is adopted but for the real and practical ramp input. The paper describes a novel approach for determining the exact analytic waveform of the RC circuit outputs for ramp inputs.

II. PROBLEM FORMULATION

Let us consider a RC circuit composed of *m*+1 number of nodes numbered from 0 to *m*. Some nodes, called input nodes, represent the initial point of a wire. These nodes connected to the output of gates, have a known voltage. Some nodes called output nodes represent the final point of a wire. They are connected to the input of a gate. Except the input and output nodes, there are internal nodes, which are not connected to gates.

Let us consider that a node i connected to the node l through a resistor R_{il} and to the node k through a capacitor c_{ik}. C_{i0} is the ground capacitor (see Figure3).



R1=R_{il}, C1 = C_{ik} and C2=C_{io}

Fig. 3. Node i connected to several nodes

Let us denote $x_i(t)$ as the voltage in time domain at the node i then,

$$\frac{1}{R_{il}}\left(x_i - x_l\right) + C_{i0}\,x_i' + C_{ik}\left(x_i' - x_k'\right) = 0 \tag{1}$$

The general form of this equation can be written as,

$$G_i\,x_i + C_i\,x_i' = \sum_{l=0}^{m} G_{il}\,x_l + \sum_{k=0}^{m} C_{ik}\,x_k' \tag{2}$$

Where, G_i is the total conductance of node i; $G_i = \sum_{l=0}^{m} 1/R_{il}$

C_i is the total capacitance of node i: $C_i = \sum_{l=0}^{m} C_{ik}$

G_{il} is the conductance between node i and l. $G_{il}=1/R_{il}$. When the nodes i and l are not connected by a resistor, G_{il} =0 (particularly G_{ii}=0).

C_{ik} is the capacitance between node i and k. When the nodes i and k are not connected by a capacitor, C_{ik} =0 (particularly C_{ii} =0).

Note that node 0 is the ground. 1 to n are the internal nodes and the output nodes. The input nodes are indexed from n+1 to m. From the general response as given in (2), a RC circuit composed of m+1 number of nodes is characterized in the time-domain by a system of n equations (S_t).

$$\left.\begin{aligned}
&G_1\,x_1(t) + C_1\,x_1'(t) = \sum_{j=0}^{m} G_{1j}\,x_j(t) + \sum_{j=0}^{m} C_{1j}\,x_j'(t)\\
&G_i\,x_i(t) + C_i\,x_i'(t) = \sum_{j=0}^{m} G_{ij}\,x_j(t) + \sum_{j=0}^{m} C_{ij}\,x_j'(t)\\
&\vdots\\
&G_n\,x_n(t) + C_n\,x_n'(t) = \sum_{j=0}^{m} G_{nj}\,x_j(t) + \sum_{j=0}^{m} C_{nj}\,x_j'(t)
\end{aligned}\right\} \tag{3}$$

Note that for each (i,j) $C_{ij}=C_{ji}$ and $G_{ij} = G_{ji}$.

It can be shown that the resolution of this system gives, for each node, the following solution.

$$x_i(t) = \sum_{k=1}^{n} a_{ik}\,e^{-h_k t} + t - \sum_{k=1}^{n} a_{ik} \tag{4}$$

Where a_{ik} is the coefficient in volt and h_k is the frequency.

III. PROPOSED MODEL

III.1 Determination of the Analytic Waveform

The method consists of resolving the system S_t. Note that no approximation is used to solve this system. First, we will consider the simple case of a RC circuit without coupling capacitance. We determine the frequencies h_k and then the coefficients a_{ik} for each node. Later, we extend the proposed method to real RC circuits with coupling capacitance.

III.2.Determining the frequencies without coupling capacitances

In order to determine the n number of frequencies we try to find n equations. A first equation is given by the value at time t=0 of the node i.

$$x_i(0)=0 \tag{5}$$

$$\sum_{k=1}^{n} a_{ik}=k \tag{6}$$

$$a_{i1}+a_{i2}+\ldots+a_{in}=k \tag{7}$$

However, the initial value of node i as well as the initial values of all the nodes of the circuit are known. Thus, we can determine the initial value of the first derivative of the node i, x'$_i$(0)

$$G_i\, x_i(t)+C_i\, x_i'(t)=\sum_{j=0}^{m} G_{ij}\; x_j(t)$$

$$x_i'(0)=\frac{1}{C_i}\left(\sum_{j=0}^{m} G_{ij}\; x_j(0)-G_i\, x_i(0)\right)=0 \tag{8}$$

On the other hand, from the expression of the node i, $x_i(t)$, we obtain,

$$x_i'(t)=-\sum_{k=1}^{n} a_{ik}h_k e^{-h_k t}+1 \tag{9}$$

$$x_i'(0)=-\sum_{k=1}^{n} a_{ik}h_k+1$$

$$\sum_{k=1}^{n} a_{ik}h_k=1 \tag{10}$$

Similarly,

$$\sum_{k=1}^{n} a_{ik}h_k^{\,2}=0;\ \sum_{k=1}^{n} a_{ik}h_k^{\,3}=0;$$

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$$\sum_{k=1}^{n} a_{ik}h_k^{\,n}=0$$

In a similar manner, we obtain a set of equations where a_{i1}, a_{i2},…, a_{in} and h_1, …, h_n are variables.

We consider the first (n+1) number of equations.

$$S_{der}=\left\{\begin{array}{l}\sum_{j=1}^{n} h_j^{\,0}a_{ij}=k;\sum_{j=1}^{n} h_j^{\,1}a_{ij}=1\sum_{j=1}^{n} h_j^{\,1}a_{ij}=0;\sum_{j=1}^{n} h_j^{\,p}a_{ij}=0;\\ \sum_{j=1}^{n} h_j^{\,n}a_{ij}=0\end{array}\right. \tag{11}$$

Unfortunately, S_{der} is a non-linear system. We try to modify this system to make it linear by eliminating the variable a_{ij}. First, a_{ij} is eliminated by subtracting the line p and the line p-1. We finally obtain n number of equations.

$$\left.\begin{array}{l}\sum_{2}^{n} h_j^{\,0}(h_j-h_1)a_{ij}=1-h_1k;\sum_{2}^{n} h_j^{\,1}(h_j-h_1)a_{ij}=-h_1\\ \sum_{2}^{n} h_j^{\,2}(h_j-h_1)a_{ij}=0;\sum_{2}^{n} h_j^{\,p-1}(h_j-h_1)a_{ij}=0\\ \sum_{2}^{n} h_j^{\,n-1}(h_j-h_1)a_{ij}=0\end{array}\right\} \tag{12}$$

In a similar manner, we proceed to the elimination of the other variables a_{ij}. After (n-1) iterations, we obtain the following equations.

$$a_{in}\prod_{j=1}^{j=n-1}(h_n-h_j)=(-1)^{n-1}\left[(h_1h_2..h_{n-2}+h_2h_3..h_{n-1}).1+(h_1h_2..h_{n-1}).k\right] \tag{13}$$

$$a_{in}h_n\prod_{j=1}^{j=n-1}(h_n-h_j)=(-1)^{n+1}(h_1h_2...h_{n-1}) \tag{14}$$

Finally, the last iteration gives,

$$0=\left\{\sum_{i=1}^{n}\ldots\sum_{L=m+1}^{n}\sum_{j=l+1}^{n}h_i...h_l...h_j\right\}.1+\prod_{i=1}^{n}h_i.k \tag{15}$$

Note that $\sigma_1=\left\{\sum_{i=1}^{n}\ldots\sum_{L=m+1}^{n}\sum_{j=l+1}^{n}h_i...h_l h_j\right\}$ (16)

$$\sigma_0=\prod_{i=1}^{n}h_i \tag{17}$$

σ_0 and σ_1 can be expressed as,

$$\sigma_1.1+\sigma_0.k=0 \tag{18}$$

Let us consider the polynomial P_n, such as

$$P_n(h)=\prod_{i=1}^{n}(h-h_i) \tag{19}$$

or, $P_n(h)=h^n+(-1)^{n-1}\sigma_1 h+(-1)^n\sigma_0$ (20)

Consequently h_i can be obtained from the roots of the polynomial $P_n(h)$. We propose a Newton Raphson based method to find the first root of P_n. Then the subsequent roots are determined iteratively by deflating P_n.

III.3 Determining the coefficients

Now, with all the coefficients h_i's are known, with the system equation as given in (13), we can determine a_{in}.

$$a_{in}\prod_{j=1}^{j=n-1}(h_n-h_j)=(-1)^{n-1}\left[(h_1h_2...h_{n-2}+h_2h_3...h_{n-1}).1+(h_1h_2...h_{n-1}).k\right] \tag{21}$$

The system S_{der} is symmetrical according to h_1, h_2… h_n. So for each K ∈ {1…, n}, we have the following equation and we can determine each coefficient a_{ik}.

$$a_{ik}\prod_{j=1}^{n}(h_k - h_j) = (-1)^{n-1}\left\{\sum_{j=1}^{n}\ldots\sum_{m=1}^{n}\sum_{l=1}^{n} h_j \ldots h_m h_l\right\} + \prod_{j=1}^{n} h_j.k; \forall j \neq k, m \neq k, l \neq k \quad (22)$$

III.4 General Case with Coupling Capacitance

The proposed method is composed of four steps. We determine the initial values of the derivatives of each node. The coefficients are σ_1 and σ_0. The frequencies h_i's are used for finding roots from $P_n(h)$. The coefficients are a_{ij}'s. When the coupling capacitor is considered for a RC circuit, determination of the derivative of the node is complex. For a node i with coupling capacitance, we have,

$$G_i\, x_i(t) + C_i\, x_i'(t) = \sum_{j=0}^{m} G_{ij}\; x_j(t) + \sum_{j=0}^{m} C_{ij}\; x_j'(t) \quad (23)$$

The computation of $x'_i(0)$ is complex one because it depends on $x'_j(0)$. In this section, we propose a method to transform the system characteristic with coupling capacitance to an equivalent system without coupling capacitance.

The initial system S_t can be written in a matrix form as,

$$GX + CX' = 0 \quad (24)$$

Where, G is the conductance matrix and C the capacitance matrix.

Note that

$$G = \begin{bmatrix} G_1 & -G_{12} & \cdots & -G_{1n} & \cdots & -G_{1m} \\ -G_{21} & G_2 & \cdots & -G_{2n} & \cdots & -G_{2m} \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ -G_{n1} & -G_{n2} & \cdots & G_n & \cdots & -G_{nm} \\ 0 & 0 & \cdots & 0 & 0 & 0 \\ 0 & 0 & \cdots & 0 & 0 & 0 \end{bmatrix} \quad (25)$$

and

$$C = \begin{bmatrix} C_1 & -C_{12} & \cdots & -C_{1n} & \cdots & -C_{1m} \\ -C_{21} & C_2 & \cdots & -C_{2n} & \cdots & -C_{2m} \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ -C_{n1} & -C_{n2} & \cdots & C_n & \cdots & -C_{nm} \\ 0 & 0 & \cdots & 0 & 0 & 0 \\ 0 & 0 & \cdots & 0 & 0 & 0 \end{bmatrix} \quad (26)$$

Without coupling capacitance, C is diagonal but with coupling capacitance the matrix is not diagonal. So, we propose to apply some addition and subtraction between lines such as the matrix C becomes diagonal. The same operations made on C have to be done on G. So, a transformed matrix equation has been obtained as given by,

$$G_{new}X + C_{new}X' = 0 \quad (27)$$

With

$$G_{new} = \begin{bmatrix} G'_1 & -G'_{12} & \cdots & -G'_{1n} & \cdots & -G'_{1m} \\ -G'_{21} & G'_2 & \cdots & -G'_{2n} & \cdots & -G'_{2m} \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ -G'_{n1} & -G'_{n2} & \cdots & G'_n & \cdots & -G'_{nm} \\ 0 & 0 & \cdots & 0 & 0 & 0 \\ 0 & 0 & \cdots & 0 & 0 & 0 \end{bmatrix} \quad (28)$$

and

$$C_{new} = \begin{bmatrix} C'_1 & 0 & \cdots & 0 & \cdots & 0 \\ 0 & C'_2 & \cdots & 0 & \cdots & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ 0 & 0 & \cdots & C'_n & \cdots & 0 \\ 0 & 0 & \cdots & 0 & 0 & 0 \\ 0 & 0 & \cdots & 0 & 0 & 0 \end{bmatrix} \quad (29)$$

Hence, the equivalent system characteristic can be written as,

$$\left.\begin{aligned} G'_1\, x_1(t) + C'_1\, x'_1(t) &= \sum_{j=0}^{m} G'_{1j}\; x_j(t) \\ S_{eq} = G'_i\, x_i(t) + C'_i\, x'_i(t) &= \sum_{j=0}^{m} G'_{ij}\; x_j(t) \\ G'_n\, x_n(t) + C'_n\, x'_n(t) &= \sum_{j=0}^{m} G'_{nj}\; x_j(t) \end{aligned}\right\} \quad (30)$$

This equivalent system does not contain any coupling capacitance. It is now possible to determine $x'_i(0)$ according to $x_i(0)$ and then to apply the method as discussed in sub-section 3.1 and 3.2.

IV. SIMULATION RESULTS AND DISCUSSIONS

A prototype tool that implements the model described in this paper has been developed. It is composed of five steps; determine the initial values and the matrix equation, compute an equivalent capacitance matrix without coupling capacitance, find the polynomial roots and calculate the coefficients.

This prototype has been tested on a 1GHZ PC machines with 1 GB RAM for two kind of RC circuits: networks with coupling capacitance with two outputs (see Figure 4) or three outputs (see Figure 5) and a variable number of internal nodes ranging from 50 to 500.

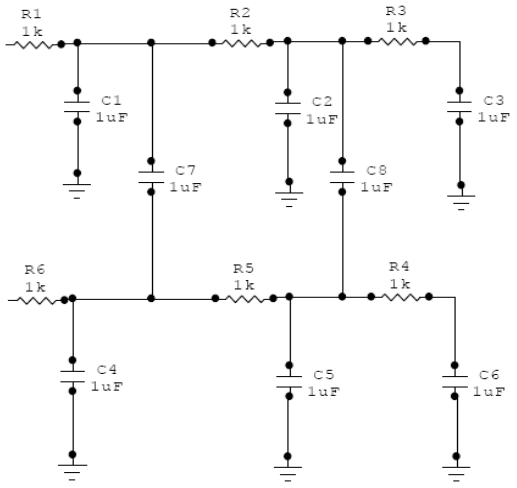

Fig. 4. Network with coupling capacitance and two outputs (All resistances have the value R and all capacitances have the value C)

The number of bits used to represent the floats and the execution time to compute the frequencies and the coefficients according to the networks are discussed in this section. It has been proved that the use of traditional float (64 bits) is not appropriate because the range of the polynomial coefficient is very important. We have used the GNU Multiple precision Arithmetic Library [5] to represent the floats with a variable number of bits. Figure 6 shows the number of bits used to represent floats for different number of internal node.

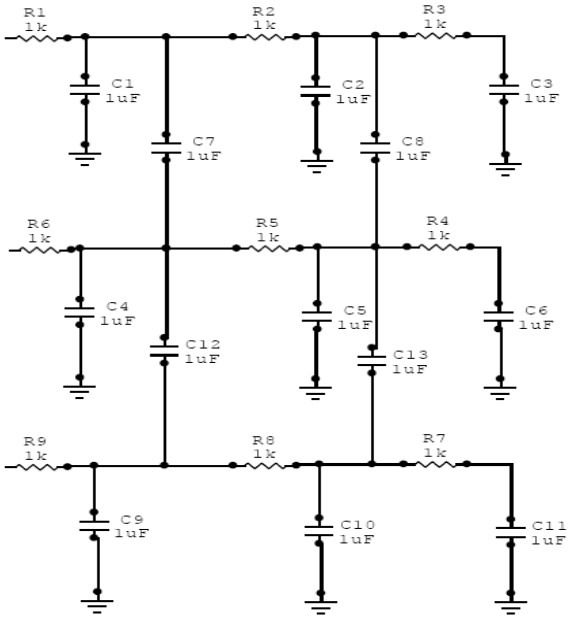

Fig.5. Network with coupling capacitance and three outputs (All resistances have the value R and all capacitances have the value C)

Note that the number of bits used to represent the floats is globally linear with the number of internal node. Figure 7 shows the execution time obtained to determine the frequencies h_j. For example, 50 sec are needed to compute the frequencies of a network with 3 outputs and 500 internal nodes. Figure 8 shows the execution time obtained to compute the coefficients a_{ij}, e.g. 25 sec are needed to compute the coefficients of a network with 3 outputs.

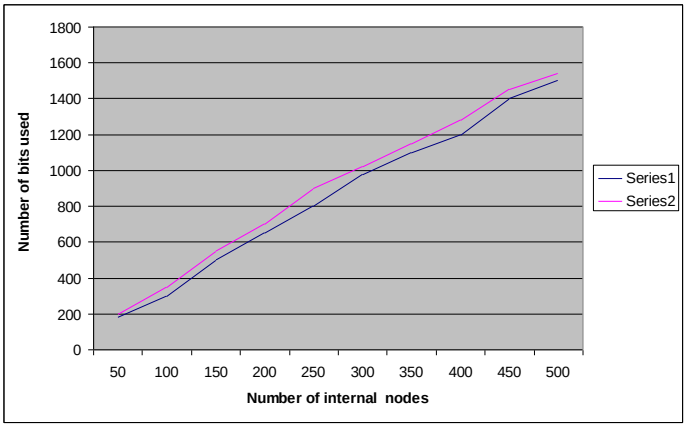

Fig. 6. Number of Bits used to Represent Floats (series1 for network with two outputs and series 2 for network with three outputs)

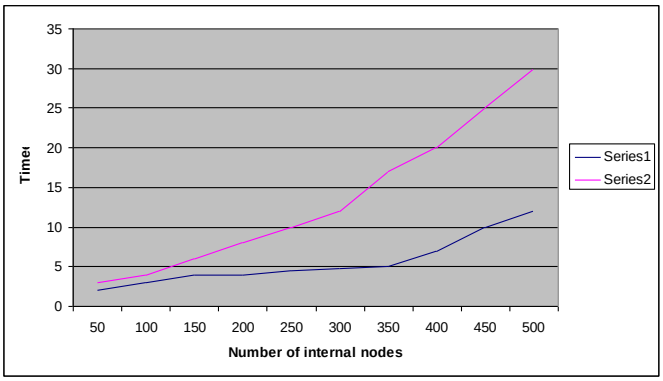

Fig.7. Execution time for determining the frequencies (series 1 for network with two outputs and series 2 for network with three outputs)

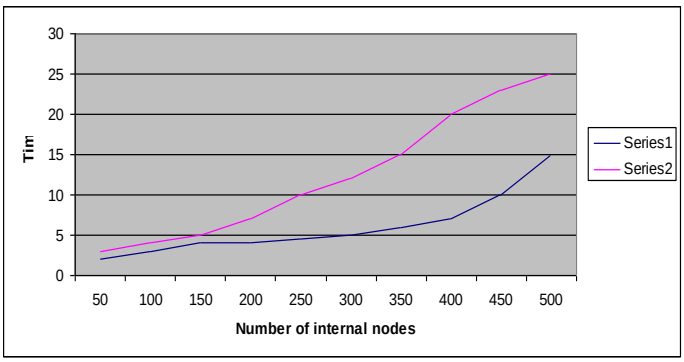

Fig.8. Execution time for determining the co-efficient (series 1 for network with two outputs and series 2 for network with three outputs)

The computation cost of the proposed method is comparable to that of the methods proposed in [1] [7] [6] [15] [10]. But, our proposed method computes and captures the system characteristic without any approximation or truncation of the exact waveform of the output according to the input and the earlier methods make some approximations and can generate an error of as high as 15%. The proposed method can

be improved with the following two directions. First, we can develop techniques to accelerate the method in decreasing the number of internal node. We can analyze the RC-circuit and merge the nodes which have the same time constant or we can split a RC-circuit in several RC sub- circuit. Thus, the analytic waveform of each output is calculated more quickly. The second improvement concerns the method. For very deep submicron processes the inductance of the interconnect can have a significant impact on the circuit. Thus, the method has to be modified to take into consideration the inductance of the interconnect.

V. CONCLUSION

Signal integrity is becoming a major issue in the verification process of high performance designs. Coupling capacitance and RC-circuit of interconnect are one of the factors that may cause timing and functional failure in the circuit. In this paper, we have presented a method for determining the analytic waveform of a coupled RC-circuit output without approximation, based on representation in the time domain. The precision is exact but the computation time is important compared to an electrical simulation. On the other hand, the electrical simulation gives numerical points where as this method gives numerical functions.

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