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CLOSED FORM SOLUTION FOR DELAY AND POWER FOR A CMOS INVERTER DRIVING RLC INTERCONNECT UNDER STEP INPUT

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Abstract
In this paper, a closed form delay and power model of a CMOS inverter driving a resistive-inductive-capacitive load is presented. The model is derived from Sakurai's alpha-power law and exhibits good accuracy. The model can be used for the design and analysis of the CMOS inverters that drive a large interconnect RLC load when considering both speed and power. Closed form expressions are also presented for the propagation delay and transition time which exhibit less than 15% error compared to the SPICE for a wide range of RLC loads. Explicit methods are also provided for modelling the short-circuit power dissipation of a CMOS inverter driving a RLC line. The average error is within 22% compared to SPICE for most practical loads. The resistive power dissipation has also been considered for various RLC loads which are accurate to within 9% to that of SPICE.

Keywords: On-Chip; Delay; Power; RLC Interconnect; VLSI

I. INTRODUCTION

As the die size of CMOS integrated circuits continue to decrease, interconnections have become increasingly significant [1]. With a linear increase in length, interconnect delay increases quadratically due to the linear increase in both interconnect resistance and capacitance [2]. Large interconnect loads not only affects the performance but also cause excessive power dissipation. A large load degrades the shape of output waveform; dissipate excessive short circuit power in the following stages loading a CMOS logic gate. Several methods have been introduced to reduce interconnect delay so that these impedances don't dominate the delay in the critical path [2-7]. Furthermore, with the introduction of portable computers, power has become an important factor in the circuit design process. Thus, power consumption must be accurately estimated for improving circuit speed when driving long interconnections. Therefore, circuit level models describing both dynamic power and, recently, short-circuit power have become increasingly important [8-11].

In this paper, an analytical expression for the transient response of a CMOS inverter driving a lumped RLC load is presented. This approach is different from [12-13], where a lumped lossless capacitive load is considered. The proposed method is the extension of [15] where, a lumped RC load is considered. Furthermore, Sakurai's alpha power law [14] is used to describe the circuit operation of the CMOS transistors rather than the classical Shichman-Hodges model [16]. The alpha power law model considers short channel behaviour, permitting increased accuracy and generality in the delay and power expressions. These expressions are used to estimate the propagation delay and rise and fall times (or transition time) of a CMOS inverter. Since the output waveform is accurately calculated, the short-circuit power [17] dissipated by the following stage can also be estimated. Furthermore, due to its simplicity, these expressions permit linear programming techniques to be used when optimizing the placement of buffers for both speed and power. Delay and power expressions for on-chip RC interconnect have been proposed in [19]. In [20], the authors have proposed a delay and power formula using 4π model. But the model is computationally complex. A number of delay models [21-23], and power models [24] have been proposed for RC interconnect. But with the increase in the frequency of operation and the wire sizes, the inductance play an important role in determining the performance of on-chip interconnects. In order to overcome these problems, this paper models the on-chip interconnect as distributed RLC segments.

This paper is organized as follows: Section 2 discusses the proposed delay model of a CMOS inverter driving a RLC load. Section 3 presents the power estimation techniques of the same inverter circuit. Section 4 shows the simulation results and finally section 5 concludes the paper.

II. PROPOSED DELAY MODEL OF A CMOS INVERTER DRIVING RLC LOAD

An analytical expression describing the behaviour of a CMOS inverter driving a lumped RLC load based on Sakurai's alpha-power law model [14] is presented. The corresponding circuit schematic is given in Figure 1.

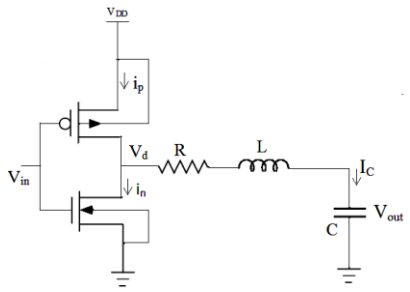


Figure 1. A CMOS Inverter Driving a RLC load

The alpha-power law model accurately describes the effects of short-channel behaviour, such as velocity saturation, while providing a tractable solution. The linear region form of alpha-power model is used to characterize the I-V behaviour of the ON transistor, since a large portion of the circuit operation occurs within this region under the assumption of a step or a fast ramp input signal. When the input to the inverter is a unit step or a fast ramp, V_{out} is initially larger than (V_{GS}-V_T) for a short period of time than for the case of a slow ramp. Therefore, the circuit operates in linear region for a greater portion of the total transition time for a large RLC interconnect load. When the load resistance is large, a large IR voltage drop occurs across the load resistor once the capacitor begins to discharge, thus V_{DS} is nearly immediately less than (V_{GS}-V_T). The N-channel device operates in the linear region once the step input goes high. However, if the input waveform increases more slowly or the load impedance is small, the inverter operates in saturation region for longer time period before switching to the linear region.

Only the falling output (rising input) waveform has been considered in this paper. The following analysis, however, is equally applicable to a rising output (falling input) waveform. The lumped load is modelled as a resistor in series with an inductor and a capacitor. The current through the output load capacitance is of same magnitude and of opposite polarity to that of the N-channel drain current (the P-channel current is ignored under the assumption of the step or fast ramp input). The capacitive current is,

$$i_c = C\frac{dV_{out}}{dt} = -i_d \qquad (1)$$

Where, C is the output capacitance, V_{out} is the voltage across the capacitance C, i_c is the current discharged from the capacitor, and i_d is the drain current through the N-channel device.

From α power law, The N-channel linear drain current is given by [14],

$$-C\frac{dV_{out}}{dt} = \frac{I_{d0}}{V_{do}}\left(\frac{V_{GS}-V_T}{V_{DD}-V_T}\right)^{\alpha} V_{DS}; \forall V_{GS} \geq V_T, V_{DS} \leq V_{GS}-V_T \qquad (2)$$

I_{d0} represents the driver current of the MOS device and is proportional to W/L, V_{d0} represents the drain-to-source voltage at which velocity saturation occurs with $V_{GS} = V_{DD}$, and is a process dependent constant, and α models the degree by which velocity saturation affects the drain to source current. $1 \leq \alpha \leq 2$, where, α=1 corresponds to a device operating strongly under velocity saturation, while α=2 represents a device with negligible velocity saturation. V_{DD} is the supply voltage, and V_T is the MOS threshold voltage (where V_{TN} (V_{TP}) is the N-channel (P-channel) threshold voltage).

Assuming a unit step input is applied to the circuit shown in Figure 1, V_{out} can be derived from (2). The linear equation, written in Laplace form is,

$$\begin{aligned} &-CsV_{out}(s) + CV_{out}(0) = \mu_{d0}V_{out}(s) + \mu_{d0}RI_c(s) + \mu_{d0}LsI_c(s) \\ &or, s^2\mu_{d0}LCV_{out}(s) + s\mu_{d0}RCV_{out}(s) + sCV_{out}(s) + \mu_{d0}V_{out}(s) \\ &= s\mu_{d0}LCV_{out}(0) + \mu_{d0}RCV_{out}(0) + CV_{out}(0) \end{aligned} \qquad (3)$$

Where, $\mu_{d0} = \frac{I_{d0}}{V_{d0}}$ is the saturation conductance.

Equation (3) yields,

$$V_{out}(t) = V_{out}(0)\left(\varsigma_1 e^{-\xi_1 t} + \varsigma_2 e^{-\xi_2 t}\right) \qquad (4)$$

Where, $\xi_{1,2} = \frac{-\gamma \pm \sqrt{\left(\gamma^2 - \frac{4}{LC}\right)}}{2}, \gamma = \frac{\mu_{d0}R+1}{\mu_{d0}L},$

$$\varsigma_1 = \frac{\gamma-\xi_1}{\xi_2-\xi_1} and \varsigma_2 = \frac{\gamma-\xi_2}{\xi_1-\xi_2}$$

Graphs of $V_{out}(t)$ for a wide range of resistive, inductive and capacitive values are shown in Figure 3. It shows that the analytical expression of output voltage as given in (4) closely approximates the SPICE result for most of the region of operation for a wide range of load impedances.

From (4), the propagation delay of a CMOS inverter can be calculated as,

$$t = \frac{\ln(\varsigma_2) + \ln\left(\frac{V_{out}(0)}{V_{out}(t)}\right)}{2\xi_1 + \xi_2} \qquad (5)$$

For 50% delay, $t_{PD} = \frac{\ln(\varsigma_2) + 0.693}{2\xi_1 + \xi_2}$ (6)

The transition time of a CMOS inverter driving a lumped RLC load calculated at the 90% point t_{tr} is,

$$t_{tr} = \frac{\ln(\varsigma_2) + 2.3}{2\xi_1 + \xi_2} \qquad (7)$$

Additional delay expressions that are used for determining short circuit power are,

$$t_{V_{TN}} = \frac{\ln(\varsigma_2) + \ln\left(\frac{V_{TN}}{V_{DD}}\right)}{2\xi_1 + \xi_2} \qquad (8)$$

$$t_{V_{TP}} = \frac{\ln(\varsigma_2) + \ln\left(\frac{V_{DD}+V_{TP}}{V_{DD}}\right)}{2\xi_1 + \xi_2} \qquad (9)$$

Equations (8) and (9) describe the time for the output voltage to change by a threshold voltage from either ground or V_{DD} for an N-channel or P-channel device, respectively.

III. PROPOSED POWER ESTIMATION TECHNIQUE

Power consumption has become one of the premier issues in VLSI circuit design. There are two primary contributions to the total transient power dissipated by a CMOS inverter, dynamic power and short-circuit power dissipation [8-11], [17-18]. The short-circuit power is often neglected, and the dynamic power is assumed to be dominant. As described below and in [8-11], [17-18], the magnitude of the short-circuit power is load dependent, and it is shown in this paper that short-circuit power can be a significant portion of the total transient power dissipation.

III.1 Dynamic Power

Dynamic power is the energy required to charge and discharge a load capacitance C and is characterized by, $CV^2 f$; where V is the source voltage and f is the switching frequency. The dynamic power is independent of the load resistance.

III.2.Short Circuit Power

This paper presents a closed form expression for modelling the short circuit power in a CMOS inverter driving RLC interconnects. The logic stage following a large RLC load may dissipate significant amount of short-circuit power due to the degraded waveform originating from the CMOS inverter driving a RLC load (Figure 2). In the region where the input signal is switching between V_{TN} and (V_{DD}+V_{TP}), a DC current path exists between V_{DD} and ground. The excess current dissipated during this region is called the short-circuit current [17]. Short-circuit current occurs due to a slow input transition, and for a balanced inverter, the peak current occurs near the middle of the input transition. An example of short-circuit current is shown by the solid line in the lower graph of Fig. 4.

The total short-circuit current I_{SC} can be estimated by approximated I_{SC} as a triangle. Therefore, the integral of I_{SC} is the area of a triangle, $\frac{1}{2} base \times height$. In terms of the short-circuit current, the height can be modelled as I_{peak} and the base can be modelled as t_{base} (Figure 4). I_{peak} is the maximum saturation current of the load transistor and depends on both V_{GS} and V_{DS}, therefore, I_{peak} is both input waveform and load dependent. t_{base} is the time during which both N-channel and P-channel transistors are turned on, permitting a DC current path to exist between V_{DD} and ground. This time occurs over the region, $V_{TN} \le V_{in} \le V_{DD} + V_{TP}$. Therefore, t_{base} is found from the difference between (8) and (9), $\left|\left(t_{V_{TP}} - t_{V_{TN}}\right)\right|$. The area defined by this triangle is $\frac{1}{2} base \times height$ models the total short-circuit current I_{SC} sourced by a CMOS inverter due to a non-step input [11].

The total short-circuit current multiplied by f and V_{DD} is the short-circuit power. The short-circuit power dissipation P_{SC} of the following stage for one transition (either rising or falling edge) can, therefore, be approximated by,

$$P_{SC} = \frac{1}{2} base \times height V_{DD} f \tag{10}$$

Subtracting (8) from (9) forms the logarithmic quotient, $t_{base} = \left|\ln\left(\frac{V_{TN}}{V_{DD}+V_{TP}}\right)\right| \frac{1}{2\xi_1 + \xi_2}$. By inserting this expression for t_{base} into (10), the short-circuit power dissipation P_{SC} of a CMOS inverter following a lumped RLC load over both the rising and falling transitions can be calculated as,

$$P_{SC} = \left|\ln\left(\frac{V_{TN}}{V_{DD}+V_{TP}}\right)\right| \frac{1}{2\xi_1 + \xi_2} I_{peak} f V_{DD} \tag{11}$$

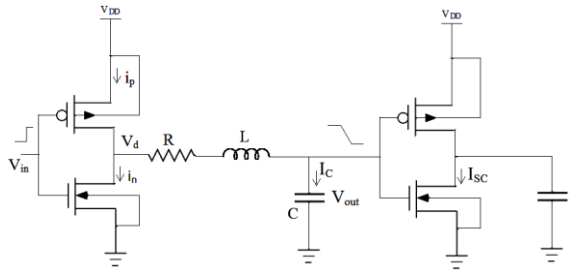


Figure 2. Non-Step Input Driving CMOS Inverter Stage Creates Short Circuit Power

III.3 Resistive Power Dissipation

In resistive interconnect, power is not only dissipated due to charging and discharging the load capacitance, but also by the load resistance. This power dissipation can be quantified by $f\int_t \left(i^2 R\right)$, where, i is the current through the load resistance. The identical current that is discharged by the load capacitor flows through the resistor. This capacitive current is $I_C = C\frac{dV_{out}}{dt}$. Therefore, by taking the derivative of (4), the instantaneous current through a resistive load $i_R(t)$ is given by,

$$i_R(t) = CV_{out}(0)\left(-\varsigma_1\xi_1 e^{-\xi_1 t} - \varsigma_2\xi_2 e^{-\xi_2 t}\right) \tag{12}$$

The average resistive power is given by,

$$P_R = fRC^2 V_{out}{}^2(0)\int_0^t \left(-\varsigma_1\xi_1 e^{-\xi_1 t} - \varsigma_2\xi_2 e^{-\xi_2 t}\right)^2 dt \tag{13}$$

Integration (13), we get,

$$P_R = fRC^2 V_{out}{}^2(0)\left[\begin{array}{l} \frac{\varsigma_1{}^2\xi_1}{2}\left(1-e^{-2\xi_1 t}\right) + \frac{\varsigma_2{}^2\xi_2}{2}\left(1-e^{-2\xi_2 t}\right) + \\ \frac{2\varsigma_1\varsigma_2\xi_1\xi_2}{\xi_1+\xi_2}\left(1-e^{-(\xi_1+\xi_2)t}\right) \end{array}\right] \tag{14}$$

IV SIMULATION RESULTS AND DISCUSSIONS

The accuracy of the analytic delay model as compared to the SPICE is tabulated in Table 1 and 2 for a wide variety of output load resistances, inductances and capacitances. Table I represents transition time and propagation delay time of a

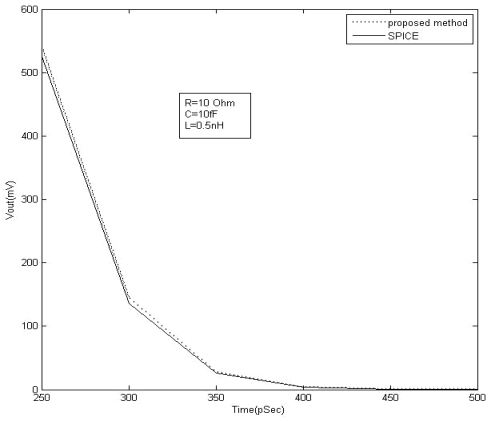
CMOS inverter driving RLC load for various R and C values for L=1nH. The average error of the transition time t_{tr} as compared with SPICE is 16.14%, and the average error of the propagation delay, t_{PD}, as compared with SPICE is 12.58%. Table 2 represents transition time and propagation delay time of a CMOS inverter driving RLC load for various R and L values for C=1pF. The average error of the transition time t_{tr} as compared to SPICE is 11.38%, and the average error of the propagation delay t_{PD} as compared to SPICE is 13.7%.

As noted above, (6) and (7) can be used to estimate the propagation delay and transition time of a CMOS inverter driving a RLC interconnects line. Since the shape of the output waveform is now known, (8) and (9) can also be used with (7) to estimate the short-circuit power dissipation of a CMOS gate loading the high impendence interconnect line, as discussed in Section 3.

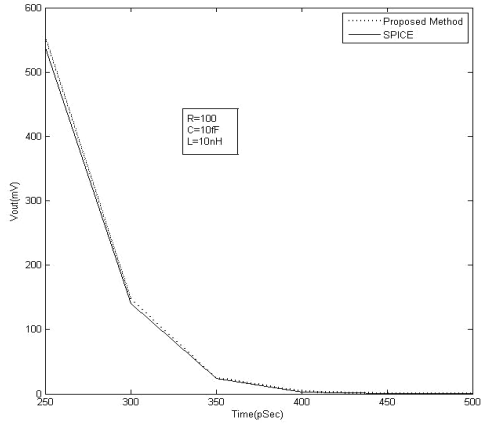
The short-circuit power derived from (11) for a wide variety of RLC loads between the CMOS inverter stages as shown in Figure 2 is compared with SPICE and given in Table 3 and 4. Table 3 shows the short circuit power dissipated by inverter circuit for various R and C values for constant L. The result is compared with SPICE and the average error is 21.7%. Table 4 presents short circuit power dissipated by inverter circuit for various R and L values for C=1fF. The result is compared with SPICE value and average error is 20.22%.

For smaller RLC loads, hence faster transition times, there is negligible short-circuit power since a direct path from power supply to ground does not exists for any significant amount of time duration. The short circuit power becomes a significant portion of total power dissipation when the CMOS inverter is loaded by larger RLC loads, creating long transition times. It is this condition that is of great interest when considering short circuit power in resistively loaded CMOS inverters. From table 3 and 4, we note that as the time constant (RC or L/R) increases, short-circuit power dissipation increases and becomes significant.

The resistive power dissipated for various RLC loads calculated from (14) is shown in table 5 and 6. Table 5 represents the resistive power dissipated by CMOS inverter driving RLC load for various R and C values for L=0.5nH. The average error is 8.49%. Note that as R is increased, the resistive power dissipation also increases. Table 6 represents resistive power dissipated by CMOS inverter driving RLC load for various R and L values for C=1fF. The estimated value is compared with SPICE result and average error is found to be as low as 4.76%.



(a)



(b)

Figure 3. Output Response of a CMOS Inverter Driving a RLC Load

TABLE I. PROPAGATION DELAY t_{PD} AND TRANSITION TIME t_{tr} OF AN INVERTER DRIVING RLC LOAD FOR L=1NH

			t_{tr} (ps)			t_{PD} (ps)		
R(Ω)	L(nH)	C(pF)	Proposed Method	SPICE	% Error	Proposed Method	SPICE	% Error
10	1nH	0.01	88.6	84.002	5.19	41	32.751	20.12
10		0.1	235.8	202.342	14.19	121	111.381	7.95
10		1	254.6	199.225	21.75	178	163.297	8.26
100		0.01	89.8	83.559	6.95	41.2	39.882	3.20
100		0.1	240	185.736	22.61	120.4	99.559	17.31
100		1	254.3	197.591	22.30	180.2	141.331	21.57
1k		0.01	101.5	88.407	12.91	44.9	37.312	16.91
1k		0.1	236.9	185.801	21.57	128.6	125.064	2.75

For a given supply voltage and frequency, dynamic power dissipation depends only on load capacitance and does not depend upon the input waveform shape or load resistance. In contrast, the short circuit power dissipation

changes with input waveform shape as well as output load resistance, inductance and capacitance. The ratio of the total transient power (sum of dynamic power and short-circuit power) of a CMOS inverter with respect to load resistance for different inductance and capacitance are given in Figure 5 and 6, respectively.

TABLE II. PROPAGATION DELAY t_{PD} AND TRANSITION TIME t_{tr} OF AN INVERTER DRIVING RLC LOAD FOR C=1PF

			t_{tr} (ps)			t_{PD} (ps)		
R(Ω)	C(pF)	L(nH)	Proposed Method	SPICE	% Error	Proposed Method	SPICE	% Error
10	1pF	0.5	248.0	197.086	20.53	182.8	142.164	22.23
100		0.5	241.1	187.552	22.21	181.8	139.698	23.01
1k		0.5	236.1	204.061	13.57	166.3	146.394	11.97
10k		0.5	151.5	128.911	14.91	145.9	127.356	12.71
10		1	254.6	239.45	5.95	192.3	150.552	21.71
100		1	242.4	222.184	8.34	187.3	148.136	20.91
1k		1	228.1	198.926	12.79	180.3	148.333	17.73
10k		1	48.0	46.757	2.59	151.3	143.417	5.21
10		10	247.1	213.717	13.51	251.5	221.370	11.98
100		10	246.2	212.274	13.78	215.9	188.373	12.75
1k		10	208.4	183.601	11.90	184.2	163.993	10.97
10k		10	131.7	123.126	6.51	180.7	174.863	3.23
10k		0.1	3.355n		2.988n		10.95	
10k		1	63.25n		57.077n		9.76	

TABLE III. ESTIMATION OF SHORT-CIRCUIT POWER DISSIPATED BY A CMOS INVERTER FOR L=0.5NH

			Power (mW), f=0.2GHz,V_{DD}=1.8V		
R(Ω)	L(nH)	C(pF)	Proposed Method	SPICE	% Error
10	0.5	0.3	25.686	19.878	22.61
10	0.5	0.5	26.748	21.144	20.95
10	0.5	1	30.146	25.821	14.35
100	0.5	0.3	25.73	20.401	20.71
100	0.5	0.5	26.932	21.925	18.59
100	0.5	1	30.532	24.819	18.71
1k	0.5	0.3	26.528	20.795	21.61
1k	0.5	0.5	29.387	23.419	20.31
1k	0.5	1	34.718	28.174	18.91

TABLE IV. ESTIMATION OF SHORT-CIRCUIT POWER DISSIPATED BY A CMOS INVERTER FOR C=1FF

			Power (mW), f=0.2GHz,V_{DD}=1.8V		
R(Ω)	L(nH)	C(fF)	Proposed Method	SPICE	% Error
10	10	1	25.553	22.337	12.586
100	10	1	25.528	20.429	19.974
10k	10	1	25.521	20.152	21.037
100k	10	1	25.499	18.939	25.726
10	40	1	25.726	20.171	21.59
100	40	1	25.585	20.132	21.313
10k	40	1	25.524	19.241	24.616
100k	40	1	70.88	60.17	15.11
10	80	1	25.783	21.551	16.414
100	80	1	25.729	20.47	20.44
10k	80	1	25.700	20.105	21.77
100k	80	1	25.52	19.876	22.117

TABLE V. RESISTIVE POWER DISSIPATED BY A CMOS INVERTER DRIVING RLC LOAD FOR L=0.5NH

		Power(Watt),f=0.2GHz,V_{DD}=1.8V		
R(Ω)	C(pF)	Proposed Method	SPICE	% Error
10	0.01	66.94f	64.296f	3.95
10	0.1	154.9f	137.536f	11.21
10	1	53.96p	49.670p	7.95
100	0.01	2.234p	2.108p	5.63
100	0.1	1.599p	1.425p	10.91
100	1	455.2p	401.714p	11.75
10k	0.01	290.3f	277.788f	4.31

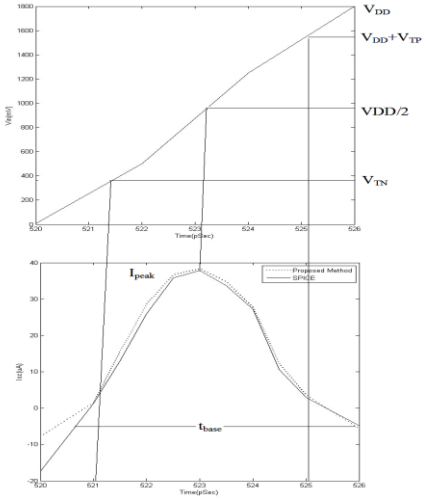


Figure 4. Short-Circuit Current for a CMOS Inverter Driving Another Inverter

TABLE VI. RESISTIVE POWER DISSIPATED BY A CMOS INVERTER DRIVING RLC LOAD FOR C=1FF

		Power(Watt),f=0.2GHz,V_{DD}=1.8		
R(Ω)	L(nH)	Proposed Method	SPICE	% Error
10	10	153f	144.417f	5.61
100	10	140.8f	129.649f	7.92
1k	10	1.08p	1.037p	3.95
10k	10	12.84p	12.235p	4.71
10	40	57.81f	55.041f	4.79
100	40	63.8f	59.43f	6.85
1k	40	167.6f	162.22f	3.21
10k	40	846.8f	820.973f	3.05
10	80	103.8f	101.599f	2.12
100	80	1.762p	1.643p	6.73
1k	80	3.718p	3.544p	4.68
10k	80	21.68p	20.919p	3.51

V. CONCLUSIONS

A simple yet accurate expression for the output voltage of a CMOS inverter driving RLC load is presented in this paper. With this expression, equations characterizing the propagation delay and transition time of a CMOS inverter driving RLC load are presented. This estimated transition time is compared with SPICE result for various R, L and C. For different R, C and constant L the average error is 16.14% and for various R, L and constant C, the average error is 11.38%. Similarly the propagation delays of CMOS inverter driving various RLC loads are estimated and are compared with SPICE. For various R, C and constant L, the average error is 12.58% and for various R, L and constant C, the average error is 13.7%. Since the output waveform of this circuit is accurately modelled, the short-circuit power dissipation of the following CMOS stage loading the interconnect line is accurately estimated and compared with SPICE. For different R, C and constant L value, the average error is 21.7% and for different R, L and constant C value, the average error is 20.22%. The resistive power dissipation is modelled and is compared with SPICE value and for different R, C and constant L value, the average error is 8.49% and for various R, L and constant C value, the average error is 4.76%. Therefore, due to the simplicity and accuracy of these expressions, the delay and power characteristics of a CMOS inverter driving high impedance RLC interconnect line can be efficiently estimated.

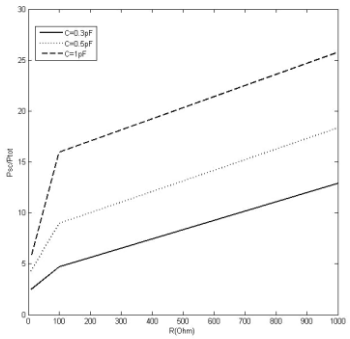


Figure 5. Ratio of Short-Circuit Power to Total Power vs Load Resistance for Different Capacitance Values and for L=0.5nH

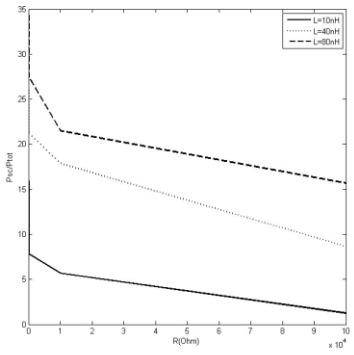


Figure 6. Ratio of Short-Circuit Power to Total Power vs Load Resistance for Different Inductance Values and for C=1fF

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