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DIFFERENTIAL VOLTAGE CURRENT CONVEYOR TRANSCONDUCTANCE AMPLIFIER BASED WAVE ACTIVE FILTER

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Abstract

This paper presents a Differential Voltage current conveyor transconductance amplifier (DVCCTA) wave active filter based on. The wave method uses emulation of reflected and incident wave for basic building block i.e. series inductor and then configuring it for other passive element realization by making appropriate connection. The functionality of the proposed method is verified for a 4th order low pass prototype filter using SPICE simulation with 0.25µm TSMC CMOS technology parameters.

Keywords: Differential voltage current conveyor transconductance amplifier, wave active filter, analog filter.

I. INTRODUCTION

Due to the potential performance features like wide bandwidth, less circuit complexity, wide dynamic range, low power consumption and high operating speed, the current mode approach for analog signal processing circuits and systems has emerged as an alternate method besides the traditional voltage mode circuits [1] The current mode active elements are appropriate to operate with signals in current or voltage or mixed mode, and are gaining acceptance as building blocks in high performance circuit designs which is clear from the availability of wide variety of current mode active elements [2-9].

The recently proposed analog building blocks in open literature are obtained by cascading of various current conveyor blocks with transconductance amplifier (TA) block in monolithic chip for compact implementation of signal processing circuits and systems. Current conveyor transconductance amplifier (CCTA) [10], [11], differential voltage current conveyor transconductance amplifier (DVCCTA) [12], are examples of such building blocks.

This paper presents systematic design approach for realization of DVCCTA based high order wave active filter. The wave active filter design is an alternative approach to the simulation of resistively terminated LC ladder filter [13-15] in the effort to obtain active RC filter of low sensitivity. In this scheme, the filter is realized by simulating the forward and reflected voltage wave present in the prototype filter. A DVCCTA based wave equivalent is developed for an inductor in series branch which can be configured for other passive element realization by making appropriate connection. A fourth order Butterworth filter has been designed using the outlined approach and the functionality has been verified through spice simulation using 0.25 μm TSMC CMOS technology parameters.

II. BASIC WAVE EQUIVALENT USING DVCCTA

II.1 DVCCTA

The DVCCTA [12] is consisting of differential amplifier, and transconductance amplifier. The port relationships of the DVCCTA as shown in Fig. 1 can be characterized by the following matrix

where g_m is the transconductance from Z terminal to O terminal of the DVCCTA. The value of g_m depend on bias current I_B and may be expressed as

$$g_m = \sqrt{2\mu_n C_{ox}(W/L)_{13,14} I_B} (2)$$

CMOS based internal circuit of DVCCTA is depicted in Fig.2.

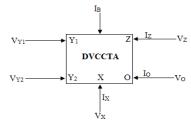


Figure 1. Schematic Symbol of DVCCTA.

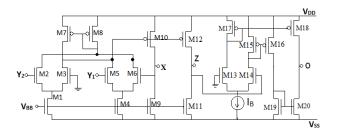


Figure 2. CMOS implementation of DVCCTA.

II.2 Basic wave equivalent

In wave method, the forward and reflected voltage waves are used to define the functionality of the filter. The incident and reflected voltage waves are depicted as A_j and B_j respectively for two port network of Fig. 3 and are related by the following relation:

$$A_j = V_j + I_j R_j, \qquad B_j = V_j - I_j R_j \tag{3}$$

Equation (3) can be expressed in terms of scattering matrix S as

$$\begin{bmatrix} B_1 \\ B_2 \end{bmatrix} = S \begin{bmatrix} A_1 \\ A_2 \end{bmatrix}$$

$$Two Port Network$$

$$V_1$$

$$V_2$$

$$V_2$$

$$V_3$$

$$V_4$$

$$V_2$$

$$V_2$$

$$V_3$$

$$V_4$$

$$V_2$$

$$V_3$$

$$V_4$$

$$V_4$$

$$V_2$$

$$V_3$$

$$V_4$$

$$V_4$$

$$V_4$$

$$V_4$$

$$V_5$$

$$V_8$$

Figure 3 Two Port Network with wave variables.

The basic element for the developing wave active filter is a series inductor L. It can be described in terms of scattering parameter as

$$S = \frac{1}{1+s\tau} \begin{bmatrix} s\tau & 1\\ 1 & s\tau \end{bmatrix} \tag{5}$$

The relationship between incident $(A_j, j=1,2)$ and the reflected wave $(B_j, j=1,2)$ of a series inductor may be obtained from (4) and (5) as

$$B_1 = A_1 - \frac{1}{1 + s\tau} \left(A_1 - A_2 \right) \tag{6}$$

$$B_2 = A_2 + \frac{1}{1 + s\tau} (A_1 - A_2) \tag{7}$$

Where $\tau = \frac{L}{2R}$ is time constant and R is represents port resistance.

The implementation of (6) and (7) require three operations - lossy integration subtraction, summation and subtraction. These operations can easily be realized using DVCCTA and are explained in the following section.

II.3 Lossy Integration

The structure to implement lossy integration subtraction is depicted in Fig. 4. It uses a single DVCCTA, a grounded capacitor and a resistor. The output voltage V_{o} is given as

$$V_o = \left(V_{in1} - V_{in2}\right) \frac{1}{1 + s\tau} \tag{8}$$

where $\tau = R_d C_d$ is time constant and $g_m R_d = 1$. Using (6), (7) and (8), the value of C_d may be computed as

$$R_d C_d = \frac{L}{2R} \quad . \tag{9}$$

Assuming $R = R_d$, the value of capacitor C_d may be expressed as

$$C_d = \frac{L}{2R^2} \tag{10}$$

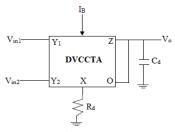


Figure 4. Lossy Integration Subtraction using DVCCTA.

Subtraction: The subtraction operation can be easily performed with DVCCTA as it has two high input impedance terminals. Fig. 5 shows the topology that can be used for voltage subtraction and the voltage output is given as

$$V_o = V_{in1} - V_{in2}$$
 with $g_m R_d = 1$ (11)

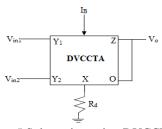


Figure 5 Subtraction using DVCCTA.

Summation: The circuit for summation is shown in Fig. 6. The first DVCCTA inverts the inputs V_{in2} which is then subtracted from input V_{in1} by second DVCCTA to provide output as

$$V_o = V_{in1} + V_{in2}$$
 with $g_m R_d = 1$ (12)

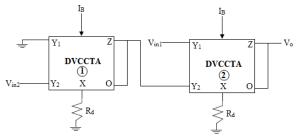


Figure. 6 Summation using DVCCTA.

The complete schematic of wave equivalent for series inductor as given by (6) and (7) can be obtained by cascading the blocks of Figs. 4 to 6. The arrangement is shown in Fig. 7(a) and its symbolic representation [13]-[15] is shown in Fig. 7(b). It may be noted that the proposed realization uses significantly lesser number of resistor than the earlier reported structures [13] – [15].

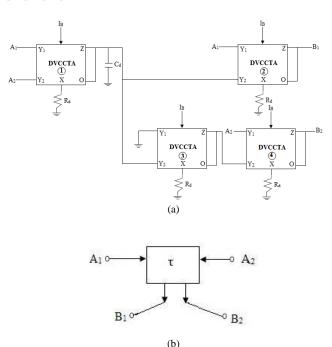


Figure 7 (a) Complete schematic of DVCCTA based wave equivalent of series inductor and (b) its symbolic representation

III. REALIZATION OF PASSIVE COMPONENTS

The structure shown in Fig. 7 can be used as the basic building block for deriving the wave equivalent of other reactive elements. The wave equivalent for series and shunt inductor and capacitor are given in Table 1 which can be obtained by swapping outputs and signal inversion. The schematic for subtraction as shown in Fig. 5 is used for signal inversion by making $V_{\rm inl} = 0$.

The design of wave active filter starts with the selection of prototype filter based on specifications. The individual inductors or capacitors are replaced by their wave

equivalents from Table 1. [13]-[15]. The complete filter schematic is then obtained by simply cascading the wave equivalents.

IV. SIMULATION RESULTS

To demonstrate the method outlined in section 2 and 3, a fourth order low pass filter of Fig. 8 has been taken as prototype. The normalized component values are $R_s = 1$, $L_1 = .7654$, $L_2 = 1.8485$, $C_1 = 1.8485$, $C_2 = .7654$ and $R_L = 1$ for maximally flat response.

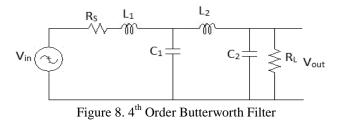


TABLE 1
Wave equivalent of Elementary Two Port consisting of single element in series and shunt branch.

Elementary two port	Port Connection	Realized Time Constant; Capacitor value for DVCCTA based wave equivalent
L	$A_1 \circ \longrightarrow \tau \longrightarrow A_2$ $B_1 \circ \longrightarrow B_2$	$\tau = \frac{L}{2R}; C_d = \frac{L}{2R^2}$
	A ₁	$\tau = 2RC; C_d = 2C$
R R	$A_1 \circ \longrightarrow T \circ A_2$ $B_1 \circ \longrightarrow B_2$	$\tau = 2L/R; \ C_d = \frac{2L}{R^2}$
$\begin{matrix} & & & \downarrow & \\ & & & \downarrow & \\ & & & \downarrow & \\ & & & &$	$\begin{array}{cccccccccccccccccccccccccccccccccccc$	$\tau = RC/2; C_d = C/2$

The wave equivalent topology of Fig. 8 may be constructed by replacing series inductor and shunt capacitor by wave equivalent of Tab. 1 and is shown in Fig.9. For cut-off frequency $f_o = 200 \text{ kH}_z$, the bias currents I_B and resistance R_d are taken as $200\mu A$ and 1447.5Ω respectively. The capacitor values for wave equivalent of series inductors (L_1 , L_2) and shunt capacitors (C_1 , C_2) are 210.379 pF, 508.082 pF and 508.082 pF, 210.3793 pF respectively. The topology of

Fig. 9 has been simulated using DVCCTA based wave equivalent and inverter as discussed in section 2 using $0.25\mu m$ TSMC CMOS technology parameters and power supply of $\pm 1.25 V$. The aspect ratios of various transistors of DVCCTA are listed in Table. 2. Figures 10 and 11 show the simulated low pass responses (V_{out}) and its complementary high pass response (V_{out}) respectively.

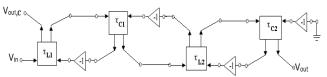


Figure 9. Wave Equivalent of prototype filter

TABLE.2 Aspect ratio of various Transistors

Transistors	Aspect ratio (W(μm)/L(μm))
$M_1, M_4, M_9, M_{11}, M_{19}$	3/0.25
M_2, M_3, M_5, M_6	1/0.25
M_7 - M_8 , M_{15} , M_{17}	5/0.25
M_{10}, M_{12}	12.5/0.25
$M_{13} - M_{14}$,	5/0.25
M_{16}	4.35/0.25
M_{18}	4.65/0.25
M_{20}	2.74/0.25

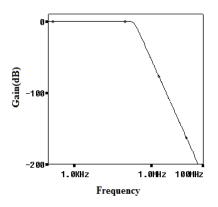


Figure 10. Frequency Response of 4th Order Low Pass Filter

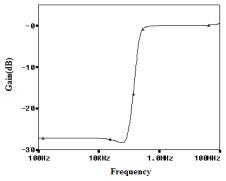


Figure 11. Frequency Response of Complementary High Pass Filter

V. CONCLUSION

New DVCCTA based high order voltage mode filter based on wave method is presented. The DVCCTA based series inductor wave equivalent is proposed as it is basic building block which is then configured for other passive element realization by making appropriate connections. The proposed structure uses grounded capacitors. The proposed approach is verified for a 4^{th} order low pass filter through SPICE simulation using $0.25\mu m$ CMOS technology parameters.

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