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LOW VOLTAGE HIGH PERFORMANCE CMOS OPERATIONAL AMPLIFIER WITH RAIL-TO-RAIL INPUT/OUTPUT STAGE

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Abstract

In this paper a low voltage constant transconductance (g_m) rail-to-rail input and output CMOS operational amplifier is presented. The rail-to-rail common mode input range is achieved by using an n-channel and a p-channel differential pair connected in parallel. The constant-g_m is achieved by using additional input differential pairs which control the tail current of the input differential pairs dynamically. The floating class AB control circuit is shifted to summing circuit, which results in a noise and offset of the amplifier. A floating current source biases the summing circuit and the class AB controls. This floating current source has the same architecture as the class AB control and provides a constant quiescent current, independent of the power supply. Special attention has been given to reduce the systematic offset voltage. Gain boost amplifiers are connected to provide not only an increase of the low frequency open loop gain but also a significant reduction of the offset voltage. Frequency compensation is performed by Cascoded Miller technique. The proposed opamp provides an open loop gain of 95.7 dB and a unity gain frequency (UGF) of 2.39 MHz.

Keywords: Low voltage, Rail-to-rail, Operational amplifier, Constant-g_m, Gain boosting, Frequency compensation.

I. INTRODUCTION

With the development of VLSI systems, designing analog integrated circuits that can operate from low supply voltages has been gaining an increasing interest in recent years. The operational amplifier which is an important building block is not an exception [1-3].

The demands for low voltage low power systems are due to the following reasons [4-5]. First, the battery operated portable devices require low power dissipation to increase battery life and minimum no of cells to reduce the volume and weight. The second reason is due to smaller sizes offered by today's VLSI technologies, which results in larger electric field. Thus it requires lower supply voltages unless this causes reliability problems. The third reason arises due to increase in packing density on silicon chip which increases the power dissipation per unit area. Hence in order to prevent overheating of the silicon chip supply voltages have to be lowered.

The input stage of an operational amplifier is the key part. The low supply voltage limits the input common mode range which should be kept as wide as possible. In order to obtain a reasonable signal-to-noise ratio and a large dynamic range, the input common mode voltage should extends from the negative supply rail to the positive supply rail i.e., rail-to-rail. This can be achieved by using an n-channel and a p-channel differential pair connected in parallel [6-7].

In this paper, a low voltage low power gain boosted rail-to-rail input and output operational amplifier is presented. The opamp consists of a constant transconductance (g_m) rail-to-rail input stage and a class AB output stage. The class AB driver circuit has been introduced. A floating current source has been used to bias the summing circuit and the class AB driver. The floating current source which has the same architecture as the class AB control resulting in a quiescent current independent of the power supply voltage. All the transistors operate in strong inversion. Frequency compensation is performed by Cascoded Miller technique in place of conventional Miller compensation. This increases the unity gain frequency (UGF) of the amplifier.

The paper is organized as follows. The constant-g_m rail-to-rail input stage and the current summing circuit with class AB output stage are described in section II and section III, respectively. In section IV and section V the gain boost amplifiers and the frequency compensation technique are discussed. Simulation results are presented in section VI and some conclusions are drawn in section VII.

II. CONSTANT-GM RAIL-TO-RAIL INPUT STAGE

When the common mode input voltage is near the positive or negative supply rail, only the n-channel or p-channel differential pair operates and in the middle range both differential pairs operate. Thus there are three distinct regions as follows:

Region I: When input common mode voltage (V_{icm}) is close to the negative supply rail, only p-channel differential pair operates. Then effective transconductance of the input stage is given

$$g_{m(eff)} = g_{mp} \quad (1)$$

Region II: When V_{icm} is in the middle range, both differential pairs operate. Then effective transconductance is given by

$$g_{m(eff)} = g_{mp} + g_{mn} \quad (2)$$

Region III: When V_{icm} is near the positive supply rail, only the n-channel differential pair operates. Then effective transconductance is given by

$$g_{m(eff)} = g_{mn} \quad (3)$$

where g_{mp} is the input transconductance for the p-channel input and g_{mn} is the input transconductance for the n-channel input.

When both the differential pairs operate, the total transconductance of the input stage is twice of that, when just one differential pair operates. Therefore, the bandwidth also changes by a factor of two. The input stage presented in this paper employs input pairs operating in strong inversion. If I_{tp} and I_{tn} indicate the tail current of the p-channel and n-channel input differential pairs, then the following relationship is required for any common mode input voltage

$$g_{m(eff)} = \sqrt{2\beta_p I_{tp}} + \sqrt{2\beta_n I_{tn}} = \text{Constant} \quad (4)$$

where $\beta_p = \mu_p C_{ox}(W/L)_p$ and $\beta_n = \mu_n C_{ox}(W/L)_n$

Here μ_p and μ_n are the carrier mobility under the channel, C_{ox} is the normalized oxide capacitance per unit area, W is the transistor gate width and L is the transistor gate length.

The input common mode range of a p-channel differential pair is restricted from the negative rail voltage to the level of positive rail voltage minus the gate-source voltage V_{gsp} of p-channel differential pair and the saturation voltage V_{dsp} of the tail current source. The common mode input range of an n-channel differential pair is restricted from the positive rail voltage down to V_{gsn} and V_{dsn} above the negative rail voltage as shown in Fig. 1. To obtain a rail-to-rail input range the supply voltage has to be at least

$$V_{sup,min} = V_{gsn} + V_{gsp} + V_{dsn} + V_{dsp} \quad (5)$$

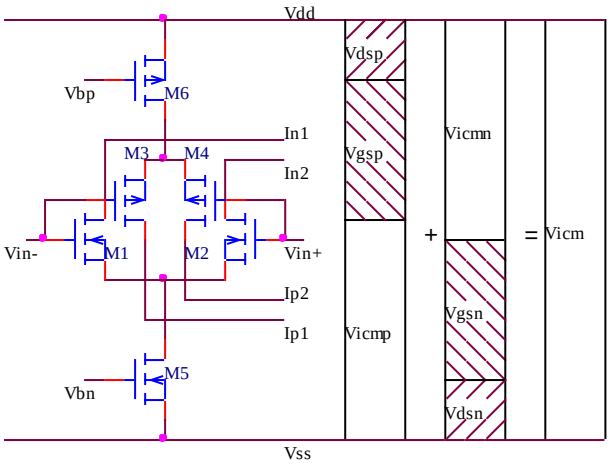


Figure 1. Rail-to-rail input stage with input common mode range.

If the p-channel and n-channel transistors are sized so that $\beta_p = \beta_n = \beta$ then equation (4) can be written as

$$g_{m(eff)} = \sqrt{2\beta} \cdot (\sqrt{I_{tp}} + \sqrt{I_{tn}}) = \text{Constant} \quad (6)$$

The constant-g_m technique can be achieved by using additional input differential pairs as shown in Fig. 2, where the drain of n-channel additional input pair M_7 and M_8 are connected to the tail current transistor M_6 of p-channel input differential pair and the drain of p-channel additional input pair M_9 and M_{10} are connected to the tail current transistor M_5 of n-channel input differential pair. Transistors M_{13} and M_{14} are used to keep the transistors M_{11} and M_{12} in triode region when the additional input differential pairs are off [8-9].

When only p-channel input pair or n-channel input pair operates, the additional input differential pairs do not have any effect. When both of the input differential pairs operate, the additional input differential pairs take away $3I_b$ of the $4I_b$ tail current. Thus when common mode input voltage (V_{icm}) is near V_{dd}, transistors M_1 and M_2 are biased at a current of $4I_b$ and when V_{icm} is near V_{ss}, transistors M_3 and M_4 are biased at the same current of $4I_b$. For the middle range of the input voltage both n-channel and p-channel input differential pairs are biased at a current of I_b.

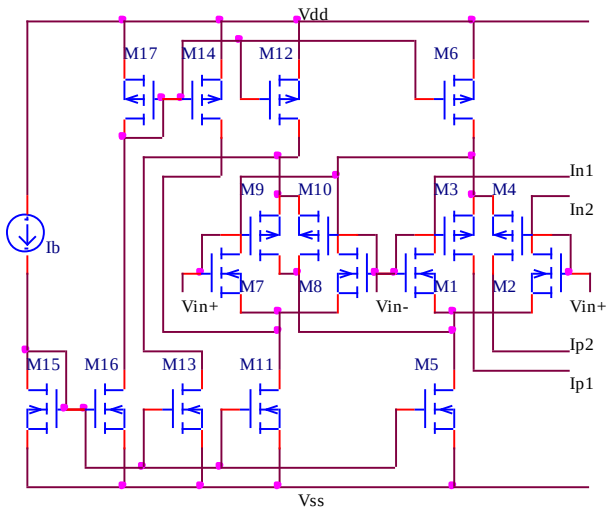


Figure 2. Rail-to-rail input stage with g_m control circuit.

Therefore the effective input transconductance of the three regions become

Region I and III:

$$g_{m(eff)} = \sqrt{2\beta(4I_b)} = 2\sqrt{2\beta I_b} \quad (7)$$

Region II:

$$g_{m(eff)} = \sqrt{2\beta I_b} + \sqrt{2\beta I_b} = 2\sqrt{2\beta I_b} \quad (8)$$

Thus equation (6) holds good for all common mode input voltages.

III. CURRENT SUMMING CIRCUIT AND THE OUTPUT STAGE

The current mirror M_{18}, M_{19} and M_{28}, M_{29} together with cascodes M_{20}, M_{21} and M_{26}, M_{27}, respectively, and a floating current source formed by M_{22} and M_{23} form the summing circuit as shown in Fig. 3. The current generated by the floating current source M_{22} and M_{23} flows through M_{20} and M_{26}. Now at the source of M_{20}, the bias current of the n-channel input pair is added and the current is mirrored by M_{18} and M_{19}. At the source of M_{21}, the bias current of the n-channel input pair is

again subtracted. Similarly at the current mirror M_{28} and M_{29} the same addition and subtraction occurs. As a result the current through M_{21}, M_{27} and the class AB driver transistors M_{24} and M_{25} is constant and equal to the current set by the floating current source. Thus the biasing of the output stage is not affected by the common mode input voltage [10-11]. The cascode stages provide the necessary level shift between the input and output stage. Also M_{21} and M_{27} provide gain by leaving the high input impedance of the gates of the output stage intact.

To achieve the rail-to-rail output voltage and for efficient use of the power supply the output transistors M_{36} and M_{37} are connected in common source configuration and they are biased in class AB configuration. The class AB biasing is in principle represented by the voltage source V_{AB} and is implemented using two complementary head-to-tail connected transistors M_{24} and M_{25}. The sum of the gate source voltages of the output stage is equal to the sum of a reference p-channel MOS gate-source voltage V_{gsp} and an n-channel MOS gate-source voltage V_{gsn} and is obtained by giving V_{AB} the values [11]

$$V_{AB} = V_{dd} - V_{ss} - V_{gsp} - V_{gsn} \quad (9)$$

At low supply voltages V_{AB} can be negative and depending on the type of class AB behavior V_{AB} may be signal independent.

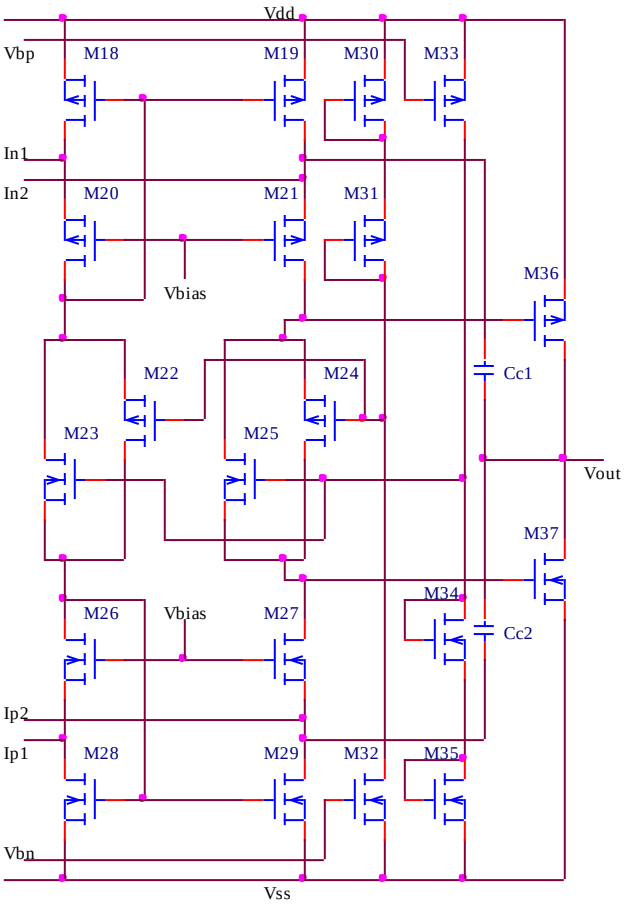


Figure 3. Integration of the output stage with first gain stage.

The class AB driver, M_{24} and M_{25}, is biased by constant current from cascodes M_{21} and M_{27} and their gate voltages are kept constant by the stacked diode connected transistors M_{30}-M_{31} and M_{34}-M_{35}. Due to the class AB control, only a small quiescent current flows through the output transistors. For large signal currents, one of the output transistors is kept at a minimum current level, while the other output transistor provides the signal current. In this situation only one of the gain boost amplifiers will contribute to the signal gain.

The integration of the class AB stage and the first gain stage has two advantages. The first advantage is due to the floating current source. Due to the floating nature of the transistors M_{22}, M_{23}, M_{24} and M_{25}, this current source contributes much less to the noise and offset of the operational amplifier. The second is that, since the floating current source M_{22} and M_{23} has the same architecture of the class AB driver circuit, M_{24}-M_{25}, the supply voltage dependency of the current mirror compensates for the supply voltage dependency of the class AB driver. The result is a quiescent current which is insensitive to variation of the supply voltage.

IV. HIGH PERFORMANCE GAIN BOOSTED OPAMP

In this section we describe an opamp which has high dc gain as well as high unity gain frequency. The opamp discussed in the previous section has high unity gain frequency. To increase its gain, the gain boosting technique can be applied to this opamp. Fig. 4 shows the gain boosting technique. The gain of a simple operational amplifier can be increased by the gain boost amplifier circuit A_{GB} by increasing the cascoding effect of the transistor M_2 without increasing the number of amplifier stage [12-14].

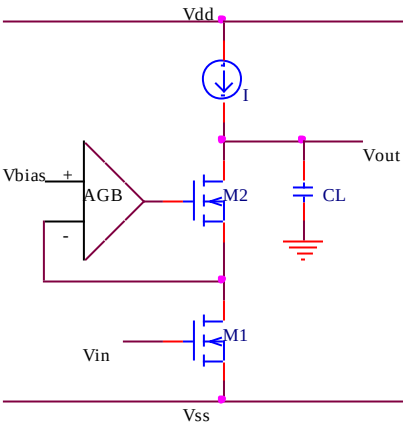


Figure 4. Cascode amplifier stage with gain boosting.

Fig. 5 shows the gain boosted class AB output stage of the proposed opamp. The output resistance of the cascode stage of Fig. 5 consisting M_{19}, M_{21} and GB_1 can be expressed as

$$R_{o,p} = A_{GB1} \cdot g_{m21} \cdot r_{o21} \cdot r_{o19} \quad (10)$$

For the other cascode stage consisting M_{27}, M_{29} and GB_2, the output resistance can be expressed as

$$R_{o,n} = A_{GB2} \cdot g_{m27} \cdot r_{o27} \cdot r_{o29} \quad (11)$$

where A_{GB1} and A_{GB2} are the dc gain of the gain boost amplifiers GB_1 and GB_2.

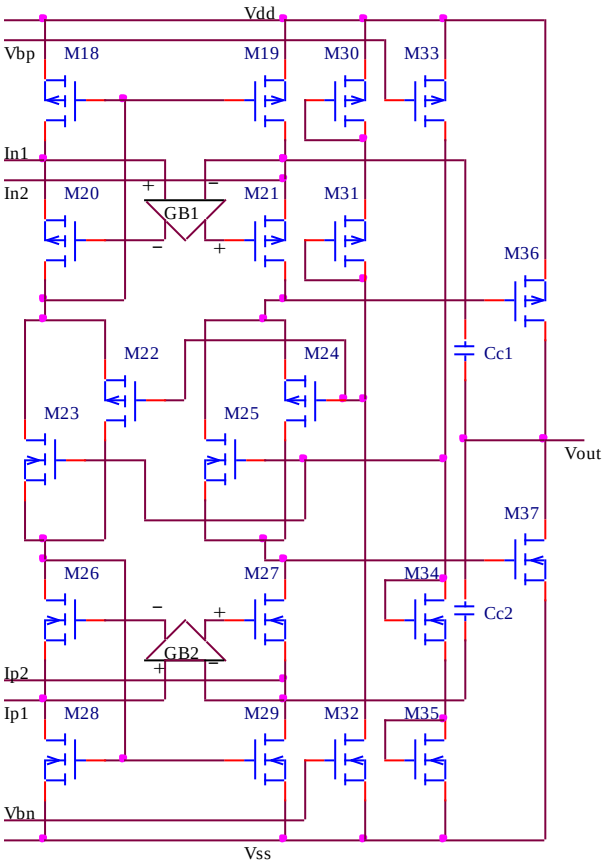


Figure 5. Gain boosted output stage of the proposed opamp.

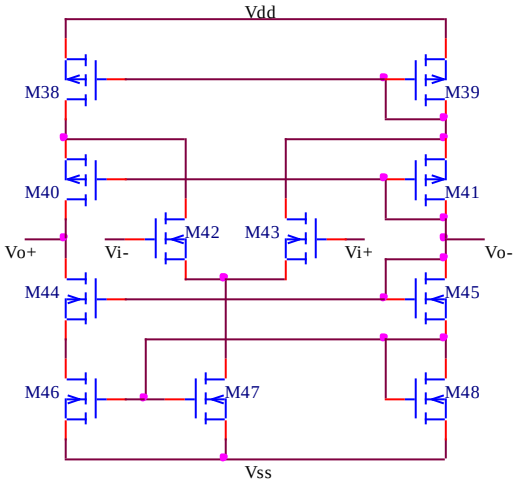
The implementation of the gain boosting amplifiers as proposed in [15-16] is shown in Fig. 6. These two non-complementary gain boosting amplifiers are self biased.

The gain of the gain boosting amplifier GB_1 is determined by the following equation

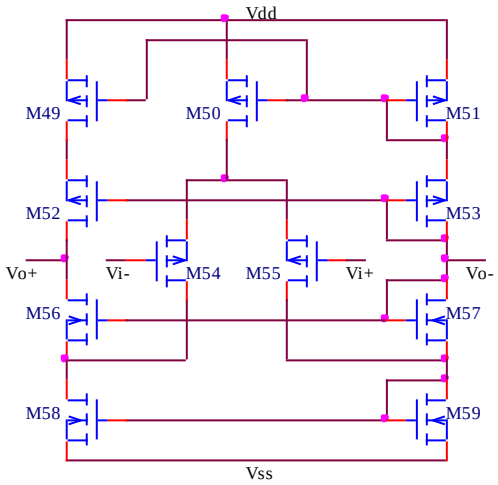
$$A_{GB1} = g_{m42} \cdot \left[(g_{m45} \cdot r_{o45} \cdot r_{o48}) \| (g_{m41} \cdot r_{o41} \cdot r_{o39})\right] \quad (12)$$

Similarly, the gain of the gain boosting amplifier GB_2 is determined by

$$A_{GB2} = g_{m54} \cdot \left[(g_{m57} \cdot r_{o57} \cdot r_{o59}) \| (g_{m53} \cdot r_{o53} \cdot r_{o51})\right] \quad (13)$$



(a)



(b)

Figure 6. Implementation of the gain boost amplifiers (a) for GB_1 and (b) for GB_2.

Hence the output resistance of the p-type cascode stage (10) can be expressed as

$$R_{o,p} = g_{m42} \cdot \left[(g_{m45} \cdot r_{o45} \cdot r_{o48}) \| (g_{m41} \cdot r_{o41} \cdot r_{o39})\right] \cdot g_{m21} \cdot r_{o21} \cdot r_{o19} \quad (14)$$

Similarly, the output resistance of the n-type cascode stage (11) can be expressed as

$$R_{o,n} = g_{m54} \cdot \left[(g_{m57} \cdot r_{o57} \cdot r_{o59}) \| (g_{m53} \cdot r_{o53} \cdot r_{o51})\right] \cdot g_{m27} \cdot r_{o27} \cdot r_{o29} \quad (15)$$

Now by designing the transistor dimension in proper way we obtain a symmetrical amplifier gain.

Usually, the non-inverting input terminal of the gain boosting amplifiers GB_1 and GB_2 are connected to a constant voltage source. Now by designing the gain boosting amplifiers as in Fig. 5, higher value of the open loop gain is achieved. This also reduces the offset voltage, because drain voltages of M_{18}, M_{19} and M_{28}, M_{29} are well matched.

V. FREQUENCY COMPENSATION

Frequency compensation is required to provide the stability of the opamp. Here frequency compensation

is performed by Cascoded Miller technique in place of the conventional Miller technique. The conventional Miller splitting shifts the output pole to a frequency given by

$$\omega_o = (g_{mo} / C_L) \quad (16)$$

where g_{mo} is the transconductance of the output transistors and C_L is the load capacitor. The Cascoded Miller compensation technique shifts the output pole to a frequency of approximately

$$\omega_o = (C_C / C_{GSout}) \cdot (g_{mo} / C_L) \quad (17)$$

Here C_C and C_{GSout} are the total compensation capacitor and the total gate-source capacitance of the output transistors [10]. Due to application of Cascoded Miller technique non-dominant pole is shifted to higher frequency position, which results to a larger unity gain frequency. For equal value of the bandwidth the amplifier employing Cascoded Miller compensation can offer higher Power Supply Rejection Ratio (PSRR) and low power consumption. The opamp with the Cascoded Miller compensation responds to small and large signal, faster than conventional Miller compensation and also gives a better slew-rate. Here Cascoded Miller compensation is performed by connecting the compensation capacitor to the source of cascode transistors M_{21} and M_{27}.

VI. RESULTS AND DISCUSSIONS

Based on the proposed constant-g_m input stage, a rail-to-rail gain boosted operational amplifier has been designed and simulated by PSpice with 0.5µm CMOS process. The threshold voltage of the n-channel and p-channel MOSFETs are in the range of 0.6 V. The supply voltage of ±1.2 V has been employed. The load is a parallel combination of 20pF capacitor and 20kΩ resistances. The open loop frequency response and the phase response of the proposed operational amplifier are shown in Fig. 7 and Fig. 8, respectively both with and without gain enhancement condition. The gain of the proposed operational amplifier increases from nearly 57.52 dB to 95.70 dB due to use of the gain enhancement circuit. The simulation results are presented in Table 1.

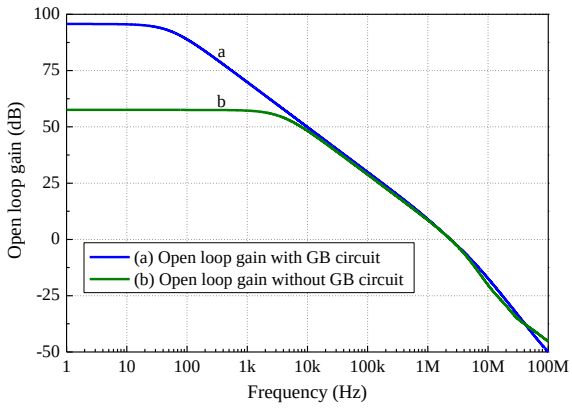


Figure 7. Open loop gain measurement both with and without gain enhancement.

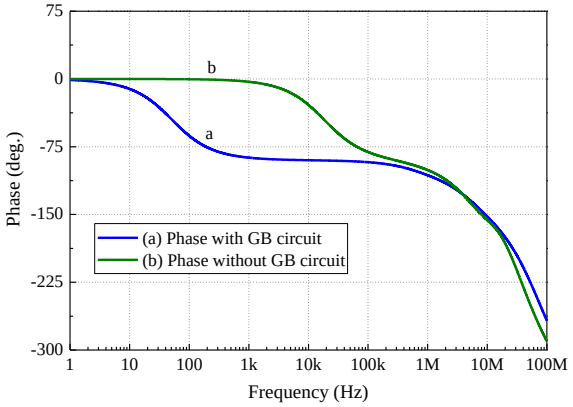


Figure 8. Phase measurement both with and without gain enhancement.

Table 1
PSpice Simulation results

Parameters	Without GB Amplifiers	With GB Amplifiers
Open loop gain	57.52 dB	95.7 dB
Unity gain frequency	2.37 MHz	2.39 MHz
Phase margin	65 deg.	62 deg.
CMRR (1kHz)	55.1 dB	66.72 dB
Slew rate	0.50 V/sec	0.51V/sec
Output noise	2.35E-11V/Hz	1.97E-11V/Hz
Power dissipation	0.81 mW	1.46 mW
Input range	Rail-to-rail	Rail-to-rail
Output range	Rail-to-rail	Rail-to-rail

VII. CONCLUSION

This paper has presented a new approach to design a constant-g_m rail-to-rail input and output CMOS operational amplifier. The amplifier contains a floating current source and specially connected gain boost amplifiers to minimize the offset voltage of the amplifier. Due to use of the gain enhancement circuit the open loop gain of the proposed operational amplifier increases from about 57.52 dB to 95.70 dB. The transistor dimensions of the gain boost amplifiers are chosen in such a way that the overall amplifier gain is symmetrical. To make efficient use of the supply current and supply voltage, power efficient class AB output stage has been used. This prevents the transistors from switching off. Here frequency compensation is performed by Cascoded Miller technique. This leads to a larger unity gain frequency compared to the conventional Miller Compensation.

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