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ANALYTICAL MODELING OF GATE CAPACITANCE OF AN ULTRA THIN OXIDE MOS CAPACITOR: A QUANTUM MECHANICAL STUDY

Amit Chaudhry[1] and Jatindra Nath Roy[2]

[1]Faculty of University Institute of Engineering and Technology, Panjab University, Chandigarh, India
amit_chaudhry01@yahoo.com

[2]Solar Semiconductor Private Limited, Hyderabad, India.

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Abstract

In this paper, an analytical model has been developed for the gate capacitance of a nanoscale metal oxide semiconductor field effect transistor (MOSFET). Both inversion layer quantization in the silicon substrate and poly silicon depletion in the gate have been included in the overall model developed. The results obtained clearly show that the gate capacitance falls due to inversion layer quantization. The results show agreement with the standard references in literature proving the validity of the model.

Keywords: Inversion layer quantization; Capacitance; Model; Poly depletion; Simulation

I. INTRODUCTION

MOSFET modeling is facing difficulties to achieve accurate description of extremely scaled down devices. The reason is that many complicated new phenomena are arising which are not easy to describe. One such phenomenon arising out of down scaling the MOSFET is the failure of classical physics at nanometer scale. As Complementary Metal Oxide Semiconductor (CMOS) technology scales down aggressively, it approaches a point, where classical physics is not sufficient to explain the behavior of a MOSFET. Due to extremely thin oxide and high doping concentration very high electrical fields at the oxide/substrate interface occur. This results in the charge carriers occupying quantized two-dimensional sub-bands which behave differently from the classical three-dimensional case [1]. Simple analytical models of the MOSFETs including quantum mechanical effects (QME) are needed for computer-aided design of digital and analog integrated circuits at nanometer scale containing thousands to millions transistors on a silicon chip. To model a MOSFET at nanoscale, the quantization of energy levels in the direction perpendicular to the oxide/silicon substrate interface, the quantum mechanical charge carrier density directly tunneling from in the gate oxide need to be properly understood and studied.

The accurate determination of capacitance voltage (CV) at nanometer scale is necessary for describing the overall MOSFET behavior. The C-V analysis for a thick oxide MOSFET is studied classically, but as the gate oxide is reduced to a few angstroms in a sub 100nm MOSFET, the electrical fields at the oxide/substrate are

increased to a large value causing discreteness of energy levels. This results in occupancy of high energy levels by the electrons causing reduced inversion charge density at the interface. The classical model suggests a maximum inversion charge density at the oxide/substrate interface. If inversion layer quantization occurs, the electron density diminishes at the interface. Through a gate capacitance model that incorporates the inversion layer quantization effect, a better understanding of the behavior of MOSFETs can be achieved.

The paper is organized as follows: The paper starts with an overview of the compact MOSFET models. Secondly, study and modeling of inversion layer quantization effect has been done. Thirdly, the poly silicon gate depletion in also modeled and included in the overall capacitance voltage analysis and finally the paper ends with conclusion and references.

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II. QUANTUM MECHANICAL CAPACITANCE VOLTAGE MODELS

Various models [1]-[7] have been reported for the calculation of C-V analysis in the presence of inversion layer quantization, but most of them are numerical in nature. These offer complex solutions and are not suitable for circuit spice simulations. So, it is important to model analytically the capacitance – voltage characteristics in all regions of inversion and depletion in the presence of inversion layer quantization.

III. INVERSIONLAYER QUANTIZATION

The nanometer-scale MOSFETs use highly-doped substrate and ultra-thin gate oxides to control short-channel effects such as drain induced barrier lowering (DIBL) and the punch through effect. All these methods used to control short channel effects result in a high electric field in the direction vertical to the silicon/silicon oxide interface. Although the high electric field in the vertical direction can keep the charges in the channel under gate control against the influence of drain potential, it confines the movement of carriers in a narrow potential well existing between the surface potential distribution and the infinite oxide potential. According to Heisenberg principle, the energy of the channel carriers can only take discrete values and not a continuous energy distribution as described by classical device physics. The silicon energy band is composed of six equal energy lobes orienting towards six directions. Every energy lobe has two directions also. One is longitudinal and the other is the transverse direction. So, the electrons present in these two directions have masses $0.916m_o$ and $0.19m_o$ respectively. Let the Si/SiO_2 interface is towards (100) direction. So, the electrons in two lobes along the interface have mass $0.916m_o$ and in the other four lobes have transverse mass $0.19m_o$ along the Si/SiO_2 interface. So, combining these four lobes of transverse mass $0.19m_o$ are grouped together and the other two lobes are grouped together as shown in figure 1. When inversion layer quantization occurs, the electrons

reside in lower energy valleys i.e. 0.916m_o mass. So, 90% of the electron population is in lower valley having longitudinal mass 0.916m_o and transverse mass 0.19m_o . Also the lower valley is slightly above the conduction band edge of the silicon conduction band as also given by Heisenberg principle. This causes a significant decrease in the inversion carrier density at a Si/SiO_2 interface in MOSFETs as compared to that of the classical case. Thus, it is important to model accurately the inversion layer quantization effect in a nanoscale MOSFET and understand the relationship between the inversion charge density and the surface potential. All the calculations done in this paper are based on the lower energy valley having longitudinal mass 0.916m_o and transverse mass 0.19m_o. The longitudinal mass 0.916m_o is used to extract the effective surface potential required to obtain inversion and transverse electron mass 0.19m_o is used for calculating the tunneling probability as explained in section IV.

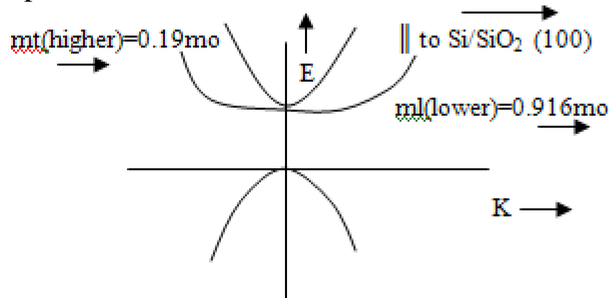

Fig 1. E-k diagram showing inversion layer lower energy and upper energy and masses in the conduction band valleys.

The research in the area of energy quantization started in the early 1950s. The research[1],[8]-[11] mainly focused on only calculating the inversion charge density in the presence of inversion layer quantization effects using variation approach and triangular well approach in the MOSFET. The use of such techniques required the calculation of surface potentials at the interface of silicon and its oxide. The lack of availability or slow development of surface potential models six decades ago, never allowed the growth of research in the area of modeling QME in MOSFETs. But as the MOSFETs are being scaled down to the nm scale, there is a need to analytically model the inversion layer quantization in nanoscale MOSFETs. Now we discuss the model, simulation and analysis of the inversion layer quantization process in the nanoscale MOSFETs. Solving the Poisson equation in the inverted channel, we get the total charge density, Q_s.

$$Q_s = -(2qN_a\varepsilon_{si}\varepsilon_0)^{1/2}\left[\varphi_s + V_t e^{-2\varphi_f/V_t}\left(e^{\varphi_s/V_t}-1\right)\right]^{1/2} \quad (1)$$

q is electron charge, ε_{si} is silicon relative permittivity, ε_0 is permittivity of free space, φ_s is surface potential, φ_f is Fermi potential, N_a is substrate concentration, and $V_t = kT/q$ is thermal voltage . Similarly, the depletion charge Q_b is approximated as

$$Q_b = -(2\varepsilon_{si}\varepsilon_0 qN_a\varphi_s)^{1/2} \quad (2)$$

Therefore, the inversion charge density Q_{inv} is given by (1) and (2):

$$Q_{\text{inv}} = -\gamma C_{\text{ox}}\left\{\left[\varphi_s + \frac{kT}{q}\exp\left(\frac{q(\varphi_s - 2\varphi_f)}{kT}\right)\right]^{1/2} - (\varphi_s)^{1/2}\right\} \quad (3)$$

γ is body effect parameter and C_{ox} is oxide capacitance (Fcm^{-2}). The main problem with (3) is that the surface-potential has to be evaluated explicitly in

all the regions of inversion and then only, (3) can be solved. An explicit solution has been evaluated in [12]. The wave function solution of the Schrödinger's equation is given by using variation approach [1]:

$$\psi(x) = \frac{b^{3/2}x}{\sqrt{2}}\exp\left(\frac{-bx}{2}\right) \quad (4)$$

b is a constant and given by

$$b = \left[\frac{48\pi^2 m^* q}{\varepsilon_{si}\varepsilon_0 h^2}\left((11/32)Q_{\text{inv}} + Q_{\text{dep}}\right)\right]^{1/3} \quad (5)$$

The (5) is then included in the explicit surface potential expression given by [13]:

$$\varphi_s = f + a \quad (6)$$

$$f = \varphi_f + 0.5\varphi_{\text{swi}} - 0.5\left[(\varphi_{\text{swi}} - 2\varphi_f)^2 + 0.0016\right]^{1/2}$$

$$a = 0.025\ \ln\left\{\left[x - y\ \left(1+100y^2\right)^{-1/2}\right]^2 \left(0.16\ \gamma\right)^{-2} - 40f + 1\right\}$$

$$\varphi_{\text{swi}} = \left[\left(V_{\text{gs}} - V_{\text{fb}} + 0.25\gamma^2\right)^{1/2} - 0.5\gamma\right]^2$$

And φ_{swi} is the weak inversion surface potential, $x = V_{\text{gs}} - V_{\text{fb}} - f$, and $y = \varphi_{\text{swi}} - f$.

The corresponding minimum energy [13] is given by

$$E_o = 3\text{h}^2 b^2 / (8m_l) \quad (7)$$

The shift in the surface potential is given as [13]

$$\Delta\varphi_s = E_0/q = 3\text{h}^2 b/(8m_l q) \quad (8)$$

The quantum surface potential is given by

$$\varphi_{\text{sqm}} = 2\varphi_{\text{f}} + \delta\varphi \quad (9)$$

Using the surface potential model (6) in (2) and (3), we can calculate explicitly inversion charge density and depletion charge density. The shift in the surface potential due to inversion layer quantization in the substrate can hence be calculated from (9). Using (9) in (3), inversion charge density using inversion layer quantization can be evaluated.

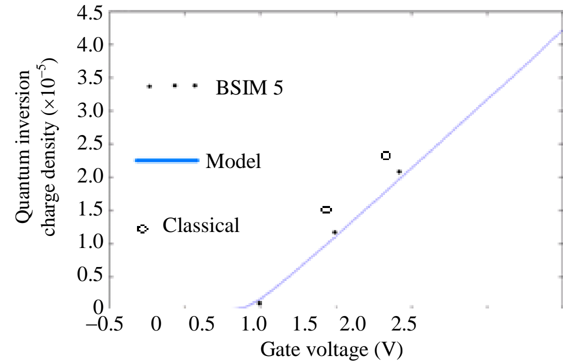

Fig. 2. Simulated results of quantum mechanical inversion charge density with gate voltage under the model parameters: substrate doping $1\text{x}10^{18}\text{cm}^{-3}$ and oxide thickness 1.5 nm.

The results in figure 2 match quite closely with the BSIM 5 results [13]. The results have been achieved by accurately modeling the shift in the surface potential. The results show that the inversion layer quantization leads to reduced inversion charge density. It has been analytically proved that the classical theory overestimates the value of inversion layer charge density as compared to the quantum mechanical charge density.

IV. GATE CAPACITANCE

Approximating the inversion charge density for the weak inversion region and strong inversion regions separately, we get after differentiating (3) with surface potential, the weak inversion and strong inversion capacitances. The MOS capacitor under inversion conditions is represented as:

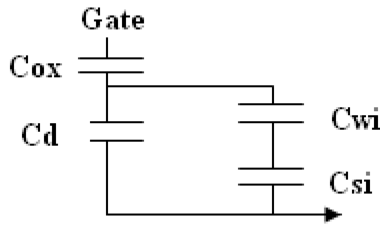

Fig. 3. Equivalent circuit of a MOS capacitor under inversion conditions.

The inversion capacitance is a series combination of weak and strong inversion capacitances.

$$C_i = C_{wi}C_{si}/(C_{si}+C_{wi}) \quad (10)$$

C_i = Inversion capacitance, $C_{wi}=(q/kT)Q_{winv}$ is the weak inversion capacitance, $C_{si}=(q/2kT)Q_{sinv}$ is the strong inversion capacitance. Q_{winv} and Q_{sinv} are the weak inversion and strong inversion charge densities, given by approximating (3) in weak and strong inversion regions. The depletion capacitance C_d is in parallel to the inversion capacitance. Therefore, the total gate capacitance

$$= C_{ox}\,(C_d + C_i) \,/\, (C_{ox} + C_d + C_i) \quad (11)$$

C_d = Depletion capacitance obtained by differentiating (2) with the surface potential, we get, $= 0.5\,\gamma_s\,C_{ox}\,\varphi_s^{-1/2}$

V. POLY SILICON DEPLETION

Poly-silicon gates are used in nanometer MOSFETs instead of metal gates in order to minimize the work function difference in the MOSFET hence to reduce the flat band voltage and hence the threshold voltage. The poly-silicon gates are of n-type in n-MOSFETs. As the gate voltage is increased, the potential drops across the poly-silicon gate also. It causes the charge carriers in the gate to get depleted and exposing the donor ions. This causes depletion in the gate and this effect is called as poly-silicon gate depletion effect as shown in figure 6. This effect is mainly caused due to the dopant penetration from the gate to the oxide thus reducing the dopant density in gate and causing larger depletion in poly gate. This potential hence, reduces the effective voltage in the oxide and the substrate. The reduced voltage in the substrate causes less inversion charge and ultimately less drain current, which is a big cause of concern for the circuits.

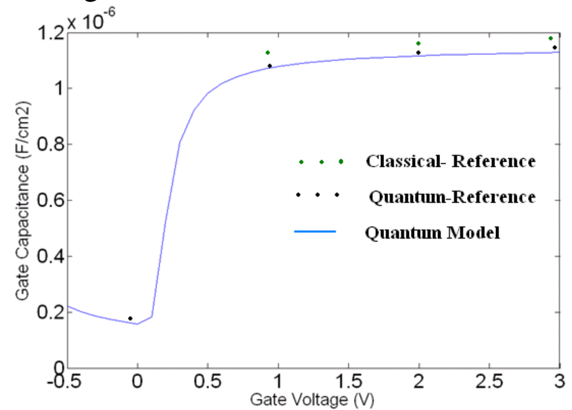

Fig 4: Simulated results of the quantum gate capacitance. The green dots show the classical gate capacitance and the black dots show the reported [14] quantum mechanical gate capacitance. The blue line shows the modeled quantum mechanical gate capacitance.

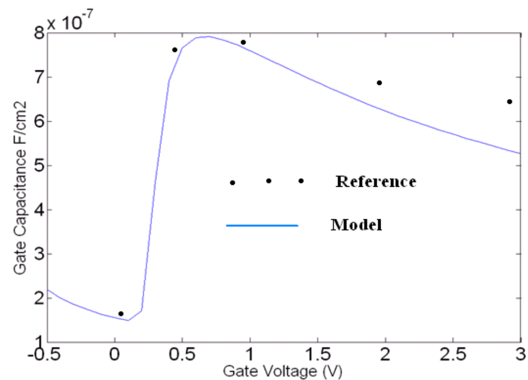

Fig 5: Simulated results of the quantum gate capacitance including depletion in poly-silicon gate. The black dots show the reported [14] quantum mechanical gate capacitance including poly depletion. The blue line shows the modeled quantum mechanical gate capacitance.

Various models [15]-[17] have already been reported to estimate the poly silicon gate depletion potential but most of them are either empirical or too complex in modeling procedure. The applied gate to source voltage is distributed across the poly silicon gate, oxide and silicon substrate as shown in figure 3.

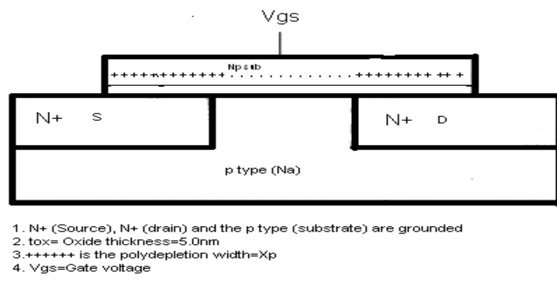

Fig 6: Poly silicon gate depletion in a MOSFET

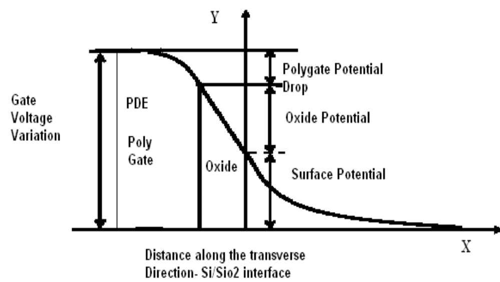

Fig 7: Variation of potential in the poly silicon gate

Applying the voltage equality at the poly silicon gate, we get

$$V_{gs} = V_{ox} + V_{fb} + \varphi_{sqm} + V_p \qquad (12)$$

V_{ox}= oxide potential, V_{fb}= flat band voltage, V_p= poly silicon gate potential. The poly silicon gate potential is also expressed in terms of polygate electrical field as

$$V_p = X_d E_p \qquad (13)$$

E_p =Electric field in the poly silicon gate and X_d = Depletion thickness in the poly silicon gate. Using gauss law by equating charges at the oxide and substrate interface, we get:

$$\varepsilon_{si} E_p = \varepsilon_{ox} E_{ox} \qquad (14)$$

ε_{ox} = relative permittivity of silicon oxide. From (12)-(14), we get

$$V_p = X_d (\varepsilon_{ox} / \varepsilon_{si})\, E_{ox} \qquad (15)$$

Also oxide electrical field

$$= \quad E_{ox} = V_{ox} / t_{ox} \qquad (16)$$

And depletion depth in uniformly doped polygate

$$X_d = (2\varepsilon_{si}\varepsilon_0 V_p / qN_{poly})^{1/2} \qquad (17)$$

And from (10) to (15), we get

$$V_p = 0.25\left[-\gamma_p + \left\{\gamma_p^{\,2} + 4\left(V_{gs} - V_{fb} - \varphi_{sqm}\right)\right\}^{1/2}\right]^2 \qquad (18)$$

γ_p =The body coefficient of poly silicon gate = $(2q\varepsilon_{si}\varepsilon_0 N_{poly})^{1/2}/C_{ox}$, N_{poly} = Polygate doping concentration. Therefore, the effective oxide capacitance is approximated as

$$C_{oxpoly} = \varepsilon_{ox}\varepsilon_0 / (X_{dp} + t_{ox}) \qquad (19)$$

Therefore, (11) becomes using (19)

$$= C_{oxpoly}\,(C_d + C_i) / (C_{oxpoly} + C_d + C_i) \qquad (18)$$

The gate capacitance has been reduced due to the inversion layer quantization

due to the reduced inversion charge densities as shown in figure 4. The parameters used for simulation are oxide thickness (t_{ox}) = 3.0nm, substrate doping (N_a) = $3x10^{17}cm^{-3}$. At gate voltage 3.0V, classical gate capacitance is more than $20pF/cm^2$ as compared to quantum mechanical gate capacitance. The poly silicon gate depletion reduces the MOSFET capacitance further. At t_{ox}=3.0nm, $N_p=5x10^{19}cm^{-2}$, $N_b=3x10^{17}cm^{-3}$, gate voltage 3.0V, the gate capacitance is around $0.53uF/cm^2$. The results in figure 5 clearly show the decrease in the gate capacitance due to poly silicon gate depletion. The results match well with the reference [14].

VI. CONCLUSION

An in-depth analytical evaluation of C-V characteristics in the presence of poly depletion and inversion layer quantization has been done. Based on the variation approach, inversion layer quantization has been modeled. The gate capacitance with QME reduces as compared to the classical gate capacitance. This is due to reduced charge density at interface of the substrate and the oxide. This is an important evaluation at nanoscale as degradation of gate capacitance can further degrade the performance of the MOSFET in all respects.

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